



SOCHIP S3 Datasheet

Video Encoding Processor

Revision 1.1

Jan.23,2018

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Sochip

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Chapter 1 About This Documentation

1.1. Documentation Overview

This documentation provides an overall description of the Sochip S3 application processor, which will provide instructions to programmers from several sections, including pin description, system, memory, image, display and interface and electrical characteristics.

1.2. Acronyms and Abbreviations

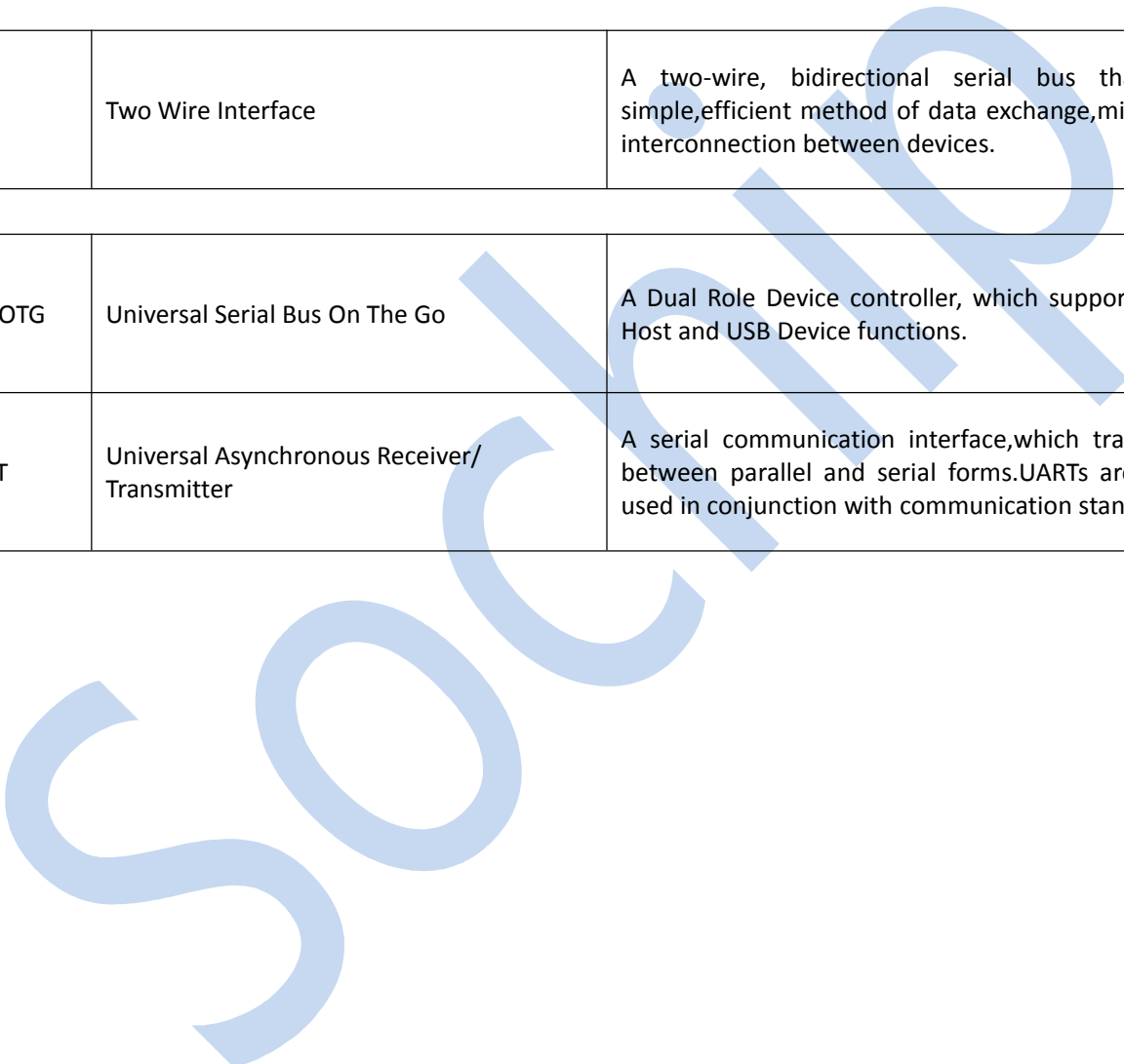
The table below contains acronyms and abbreviations used in this document.

| A | | |
|-----|------------------------------|--|
| AES | Advanced Encryption Standard | A specification for the encryption of electronic data established by the U.S. National Institute of Standards and Technology (NIST) in 2001 |
| AGC | Automatic Gain Control | An adaptive system found in electronic devices that automatically controls the gain of a signal: the average output signal level is fed back to adjust the gain to an appropriate level for a range of input signal levels |
| AHB | AMBA High-speed Bus | A bus protocol introduced in Advanced Microcontroller Bus Architecture version 2 published by ARM Ltd company |
| APB | Advanced Peripheral Bus | APB is designed for low bandwidth control accesses, which has an address and data phase similar to AHB, but a much reduced, low complexity signal list (for example no bursts) |
| AVS | Audio Video Standard | A compression standard for digital audio and video |
| C | | |
| CRC | Cyclic Redundancy Check | A type of hash function used to produce a checksum in order to detect errors in data storage or transmission |
| CSI | CMOS Sensor Interface | The hardware block that interfaces with different image sensor interfaces and provides a standard output that can be used for subsequent image processing |

| | | |
|------|---------------------------------------|---|
| D | | |
| DES | Data Encryption Standard | A previously predominant algorithm for the encryption of electronic data |
| DLL | Delay-Locked Loop | A digital circuit similar to a phase-locked loop (PLL), with the main difference being the absence of an internal voltage-controlled oscillator, replaced by a delay line |
| DRC | Dynamic Range Compression | It reduces the volume of loud sounds or amplifies quiet sounds by narrowing or "compressing" an audio signal's dynamic range. |
| DVFS | Dynamic Voltage and Frequency Scaling | Dynamic voltage scaling is a power management technique where the voltage used in a component is increased or decreased, depending on circumstances. Dynamic frequency scaling is a technique whereby the frequency of a microprocessor can be automatically adjusted on the fly so that the power consumption or heat generated by the chip can be reduced. These two are often used together to save power in mobile devices. |
| E | | |
| EHCI | Enhanced Host Controller Interface | The register-level interface for a Host Controller for the USB Revision 2.0. |
| eMMC | Embedded Multi-Media Card | An architecture consisting of an embedded storage solution with MMC interface, flash memory and controller, all in a small BGA package. |
| F | | |
| FBGA | Fine Ball Grid Array | FBGA is based on BGA technology, but comes with thinner contacts and is mainly used in SoC design |
| G | | |
| GIC | Generic Interrupt Controller | A centralized resource for supporting and managing interrupts in a system that includes at least one processor |
| I | | |
| I2S | Inter IC Sound | An electrical serial bus interface standard used for connecting digital audio devices together |
| L | | |

| | | |
|-------|--------------------------------------|---|
| LSB | Least Significant Bit | The bit position in a binary integer giving the units value, that is, determining whether the number is even or odd. It is sometimes referred to as the right-most bit, due to the convention in positional notation of writing less significant digits further to the right. |
| LRADC | Analog to Digital Converter | Used for KEY Application |
| M | | |
| MAC | Media Access Control | A sublayer of the data link layer, which provides addressing and channel access control mechanisms that make it possible for several terminals or network nodes to communicate within a multiple access network that incorporates a shared medium, e.g. Ethernet. |
| MII | Media Independent Interface | An interface originally designed to connect a fast Ethernet MAC-block to a PHY chip, which now has been extended to support reduced signals and increased speeds. |
| MIPI | Mobile Industry Processor Interface | MIPI alliance is an open membership organization that includes leading companies in the mobile industry that share the objective of defining and promoting open specifications for interfaces inside mobile terminals. |
| MSB | Most Significant Bit | The bit position in a binary number having the greatest value, which is sometimes referred to as the left-most bit due to the convention in positional notation of writing more significant digits further to the left |
| N | | |
| NTSC | National Television System Committee | An analog television system that is used in most of North America, and many other countries |
| O | | |
| OHCI | Open Host Controller Interface | A register-level interface that enables a host controller for USB to communicate with a host controller driver in software |
| P | | |
| PAL | Phase Alternating Line | An analogue television color encoding system used in broadcast television systems in many countries |
| PCM | Pulse Code Modulation | A method used to digitally represent sampled analog signals |

| | | |
|---------|--|---|
| PID | Packet Identifier | Each table or elementary stream in a transport stream is identified by a 13-bit packet ID (PID). A demultiplexer extracts elementary streams from the transport stream in part by looking for packets identified by the same PID. |
| S | | |
| SPI | Synchronous Peripheral Interface | A synchronous serial data link standard that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. |
| T | | |
| TWI | Two Wire Interface | A two-wire, bidirectional serial bus that provides simple,efficient method of data exchange,minimizing the interconnection between devices. |
| U | | |
| USB OTG | Universal Serial Bus On The Go | A Dual Role Device controller, which supports both USB Host and USB Device functions. |
| UART | Universal Asynchronous Receiver/ Transmitter | A serial communication interface,which translates data between parallel and serial forms.UARTs are commonly used in conjunction with communication standards. |



Chapter 2 Overview

The S3 processor represents Sochip's latest achievement in video encoding processors, which integrates a single ARM Cortex™-A7 CPU that operates at speed up to 1.2GHz with supporting numerous peripherals.

H.264 encoder by 1080p@60fps enables the S3 to capture superior shots in motion with the fine details. To enrich camera feature and enhance image quality, S3 equips an 8M HawkView™ ISP with advanced features like spatial de-noise, chrominance de-noise, zone-based AE/AF/AWB statistics, black level correction, lens shading correction, color correction and anti-flick detection statistics. Audio subsystem includes audio codec with dedicated hardware, and supports I2S/PCM interface for connecting to an external audio codec.

The S3 processor includes one built-in DDR3, and external memory interfaces to SPI NAND/Nor flash and SD/MMC.

Designed to be a connected solution, the S3 supports WiFi or 3G/4G connectivity to enable to be controlled wirelessly from a smartphone or other remote device. Time lapse photography is also supported by the S3 processor. To reduce total system cost and enhance overall functionality, the S3 has a broad range of hardware peripherals such as UART, SPI, USB HS/FS OTG, TWI, EMAC etc.

Applications:

- Action Camera
- CDR

2.1. Processor Features

2.1.1. CPU Architecture

- ARM Cortex™-A7 MPCore™ Processor
- Thumb-2 Technology
- Support NEON Advanced SIMD(single instruction multiple data)instruction for acceleration of media and signal processing functions
- Support Large Physical Address Extensions(LPAE)
- VFPv4 Floating Point Unit
- 32KB L1 Instruction cache and 32KB L1 Data cache
- 128KB L2 cache

2.1.2. Memory Subsystem

2.1.2.1. Boot ROM

- On-chip memory
- Size:32KB
- Support system boot from the following devices:
 - SPI Nor flash
 - SPI Nand flash
 - SD/TF card
 - eMMC flash
- Support system code download through USB OTG

2.1.2.2. SDRAM

- One built-in DDR3 memory ,Density 128MB

2.1.2.3. SD/MMC Interface

- Up to three SD/MMC controllers
- 1/4/8-bit SD,SDIO,MMC mode
- Complies with eMMC standard specification V4.41, SD physical layer specification V2.0, SDIO card specification V2.0
- Support hardware CRC generation and error detection
- Support block size from 1 to 65535 bytes

2.1.3. System Peripheral

2.1.3.1. Timer

- Three on-chip timers with interrupt-based operation
- One watchdog to generate reset signal or interrupts

- 33 bits Audio/Video Sync(AVS) Counter
- 24MHz or Internal OSC clock input

2.1.3.2. High Speed Timer

- Up to two high speed timers
- Counters up to 56 bits
- Clock source is synchronized with AHB1 clock, much more accurate than other timers

2.1.3.3. GIC

- Support 16 SGIs(Software Generated Interrupt), 16 PPIs(Private Peripheral Interrupt) and 125 SPIs(Shared Peripheral Interrupts)

2.1.3.4. DMA

- Up to 8-channel DMA
- Flexible data width of 8/16/32 bits
- Support linear and IO address modes
- Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

2.1.3.5. CCU

- 9 PLLs
- One on-chip RC oscillator
- One 24MHz oscillator
- One 32.768KHz external oscillator
- Clock management: clock gating ,clock enabling to the device modules, clock reset, clock generation, clock division

2.1.3.6. PWM

- Up to two PWM channels
- Support outputting two kinds of waveform: continuous waveform and pulse waveform
- 0% to 100% adjustable duty cycle
- Up to 24MHz output frequency

2.1.3.7. RTC

- Time,calendar
- Counters second,minutes,hours,day,week,month and year with leap year generator
- Alarm:general alarm and weekly alarm
- One 32KHz fanout

2.1.3.8. LRADC

- 6-bit resolution
- Up to two channels
- Support hold key and continuous key
- Support single key, normal key and continuous key

2.1.3.9. Security Engine

- Crypto engine
 - Support AES 128/192/256-bit with ECB,CBC,CTS,CTR mode
 - Support DES/TDES with ECB,CBC,CTR mode
 - Support SHA1 and MD5
 - 160-bit hardware PRNG with 175-bit seed
- 256-bits EFUSE

2.1.4. Display Subsystem

2.1.4.1. DE2.0

- Output size up to 1024x1024
- Support three alpha blending channel for main display
- Support four overlay layers in each channel, and has a independent scale
- Support potter-duff compatible blending operation
- Support input format YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565

2.1.4.2. Display Output

- Support LVDS interface with single link, up to 1024x768@60fps
- Support RGB interface with DE/SYNC mode, up to 1024x768@60fps
- Support serial RGB/dummy RGB/CCIR656 interface, up to 800x480@60fps
- Support i80 interface with 18/16/9/8 bit, support TE, up to 800x480@60fps
- Support pixel format: RGB888, RGB666 and RGB565
- Dither function from RGB666/RGB565 to RGB888
- Gamma correction with R/G/B channel independence

2.1.5. Video Engine

2.1.5.1. Video Decoding

- Support video decoder for H.264 and JPEG/MJPEG
- Support H.264 BP/MP/HP up to 1080p@60fps
- Support H.264 output formats :NV21,NV12,YU12,YV12
- Support JPEG/MJPEG up to 1080p@30fps

2.1.5.2. Video Encoding

- Support H.264 video encoding up to 1080p@60fps, 720p@120fps
- JPEG baseline: picture size up to 8192x8192
- Support input picture size up to 4800x4800
- Support input formats: YU12/YV12/NV12/NV21/YUYV/YVYU/UYVY/VYUY
- Support Alpha blending
- Support thumb generation
- Support 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio
- Support rotated input

2.1.6. Image Subsystem

2.1.6.1. Image Input

- Support 8/10/12-bit CMOS sensor parallel interface
- Support 8-bit CCIR656 protocol for NTSC and PAL
- Support ITU-R BT 1120 protocol for HD-CIF system
- Support 16bit interface with separate syncs
- Support MIPI-CSI2 interface compliant with MIPI-DPHY v1.0 and MIPI-CSI2 v1.0
- Support MIPI-CSI2 1/2/3/4 data lanes configuration
- Support Format:
 - YUV422-8/10 bit
 - YUV420-8/10bit(for MIPI-CSI2 only)
 - RAW-8/10/12bit
 - RGB888/RGB565(for MIPI-CSI2 only)
- Performance:
 - Still capture resolution up to 5M with parallel interface
 - Video capture resolution up to 1080p@30fps with parallel interface
 - Still capture resolution up to 8M with MIPI-CSI2 interface
 - Video capture resolution up to 1080p@60fps with MIPI-CSI2 interface
 - MIPI-DPHY maximum data rate up to 1Gbps per lane

2.1.6.2. ISP

- Support input formats:8/10-bit RAW RGB,8-bit YCbCr
- Support output formats: YCbCr420 semi-planar,YCrCb420 semi-planar, YCbCr422 semi-planar,YCrCb422 semi-planar,YUV420 planar,YUV422 planar
- Support image mirror flip and rotation
- Support two output channels
- Speed up to 8MPixels@24fps
- Defect pixel correction
- Super lens shading correction
- Anisotropic non-linear Bayer interpolation with false color suppression
- Programmable color correction
- Advanced contrast enhance and sharpening
- Advanced saturation adjust
- Advanced spatial(2D) de-noise filter
- Advanced chrominance noise reduction
- Zone-based AE/AF/AWB statistics

- Anti-flick detection statistics
- Histogram statistics

2.1.7. Audio Subsystem

2.1.7.1. Audio Codec

- Two audio digital-to-analog(DAC) channels
- Two audio analog-to-digital(ADC) channels
 - 92dB SNR@A-weight
 - Supports ADC Sample Rates from 8KHz to 48KHz
- Support analog/digital volume control
- Two low-noise analog microphone bias outputs
- Analog low-power loop from microphone to headphone outputs
- Support Dynamic Range Controller adjusting the DAC playback output(DRC)
- Four audio inputs:
 - Three differential microphone inputs
 - Stereo Linein input
- Two audio outputs:
 - Stereo Headphone output
 - Differential Lineout output
- Support Automatic Gain Control(AGC) and Dynamic Range Control(DRC) adjusting the ADC recording input

2.1.7.2. I2S/PCM

- Compliant with standard Inter-IC sound(I2S) bus specification
- Compliant with left-justified, right-justified, PCM mode, and TDM(Time Division Multiplexing) format
- Full-duplex synchronous work mode
- Master and slave mode configured
- Adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8KHz to 192KHz
- Support 8-bit u-law and 8-bit A-law companded sample

2.1.8. External Peripherals

2.1.8.1. USB

- One USB 2.0 OTG controller with PHY
- Complies with USB2.0 Specification
- Support High-Speed(HS,480Mbps),Full-Speed(FS,12Mbps),and Low-Speed(LS,1.5Mbps) in host mode
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0,and the Open Host Controller Interface(OHCI) Specification,Version 1.0a for host mode
- Up to 8 User-Configurable Endpoints in device mode
- Support point-to-point and point-to-multipoint transfer in both host and peripheral mode

2.1.8.2. Ethernet

- Integrated an internal 10/100M PHY
- Support RGMII/MII/RMII interface
- Support 10/100/1000Mbps data transfer rate
- Support full-duplex and half-duplex operation
- Support linked-list descriptor list structure
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Support a variety of flexible address filtering modes

2.1.8.3. UART

- Up to three UART controllers
- 64-Bytes Transmit and receive data FIFOs for all UART
- Compliant with industry-standard 16550 UARTs
- Support Infrared Data Association(IrDA) 1.0 SIR

2.1.8.4. SPI

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Support single and dual read mode
- Two 64-Bytes FIFO for SPI-TX and SPI-RX operation
- DMA-based or interrupt-based operation
- SPI_Clock(SPI_CLK) are configurable

2.1.8.5. TWI

- Up to two Two Wire Interface(TWI)controllers
- Support Standard mode(up to 100 Kbit/s) and Fast mode(up to 400 Kbit/s)
- Master/slave configurable
- Allows 10-bit addressing transactions

2.1.9. Package

- FBGA 234 balls, 0.65mm ball pitch, 11mm x 11mm

2.2. System Block Diagram

Figure 2-1 shows the block diagram of the S3.

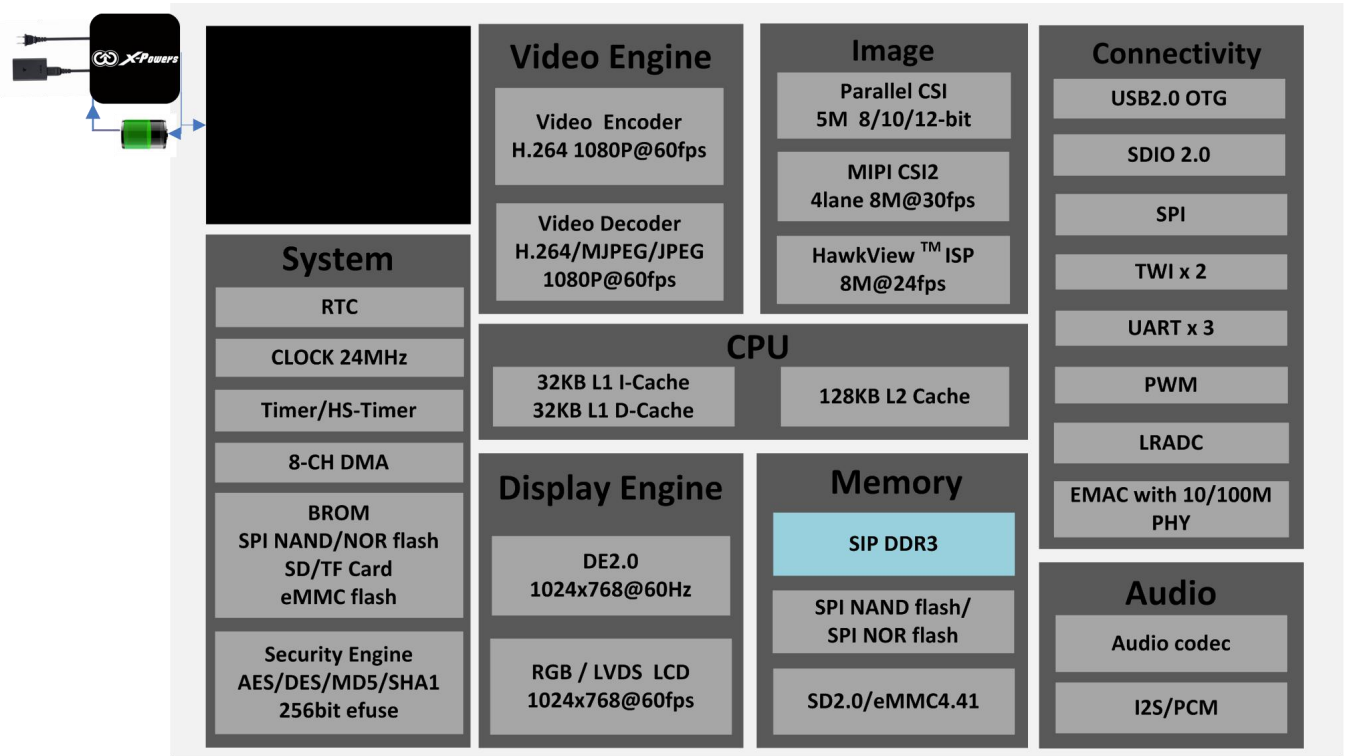


Figure 2-1. S3 Block Diagram

Chapter 3 Pin Description

3.1. Pin Characteristics

Table 3-1 lists the characteristics of S3 pins from seven aspects: BALL#, Pin Name, Default Function, Type, Reset State, Default Pull Up/Down, and Buffer Strength.

Table 3-1. Pin Characteristics

| Ball# | Pin Name | Default Function | Type | Reset State | Default Pull Up/Down | Buffer Strength (mA) |
|---------------|----------|------------------|------|-------------|----------------------|----------------------|
| GPIO B | | | | | | |
| B3 | PB0 | GPIO | I/O | Z | NO PULL | 20 |
| B4 | PB1 | GPIO | I/O | Z | NO PULL | 20 |
| B8 | PB2 | GPIO | I/O | Z | NO PULL | 20 |
| C4 | PB3 | GPIO | I/O | Z | NO PULL | 20 |
| C8 | PB4 | GPIO | I/O | Z | NO PULL | 20 |
| C7 | PB5 | GPIO | I/O | Z | NO PULL | 20 |
| A7 | PB6 | GPIO | I/O | Z | NO PULL | 20 |
| B7 | PB7 | GPIO | I/O | Z | NO PULL | 20 |
| B6 | PB8 | GPIO | I/O | Z | NO PULL | 20 |
| C6 | PB9 | GPIO | I/O | Z | NO PULL | 20 |
| A5 | PB10 | GPIO | I/O | Z | NO PULL | 20 |
| C5 | PB11 | GPIO | I/O | Z | NO PULL | 20 |
| B5 | PB12 | GPIO | I/O | Z | NO PULL | 20 |
| A2 | PB13 | GPIO | I/O | Z | NO PULL | 20 |
| GPIO C | | | | | | |
| A3 | PC0 | GPIO | I/O | Z | NO PULL | 20 |
| B2 | PC1 | GPIO | I/O | Z | NO PULL | 20 |
| B1 | PC2 | GPIO | I/O | Z | NO PULL | 20 |
| C2 | PC3 | GPIO | I/O | Z | Pull-Up | 20 |
| F3 | PC4 | GPIO | I/O | Z | Pull-Up | 20 |
| F4 | PC5 | GPIO | I/O | Z | NO PULL | 20 |
| C1 | PC6 | GPIO | I/O | Z | Pull-Up | 20 |
| C3 | PC7 | GPIO | I/O | Z | Pull-Up | 20 |
| D3 | PC8 | GPIO | I/O | Z | NO PULL | 20 |
| D2 | PC9 | GPIO | I/O | Z | NO PULL | 20 |
| D1 | PC10 | GPIO | I/O | Z | NO PULL | 20 |
| GPIO D | | | | | | |
| K15 | PD0 | GPIO | I/O | Z | NO PULL | 20 |

| Ball# | Pin Name | Default Function | Type | Reset State | Default Pull Up/Down | Buffer Strength (mA) |
|---------------|----------|------------------|------|-------------|----------------------|----------------------|
| C11 | PD1 | GPIO | I/O | Z | NO PULL | 20 |
| J14 | PD2 | GPIO | I/O | Z | NO PULL | 20 |
| J15 | PD3 | GPIO | I/O | Z | NO PULL | 20 |
| B16 | PD4 | GPIO | I/O | Z | NO PULL | 20 |
| C16 | PD5 | GPIO | I/O | Z | NO PULL | 20 |
| B9 | PD6 | GPIO | I/O | Z | NO PULL | 20 |
| A9 | PD7 | GPIO | I/O | Z | NO PULL | 20 |
| C15 | PD8 | GPIO | I/O | Z | NO PULL | 20 |
| L15 | PD9 | GPIO | I/O | Z | NO PULL | 20 |
| A15 | PD10 | GPIO | I/O | Z | NO PULL | 20 |
| B15 | PD11 | GPIO | I/O | Z | NO PULL | 20 |
| B14 | PD12 | GPIO | I/O | Z | NO PULL | 20 |
| A14 | PD13 | GPIO | I/O | Z | NO PULL | 20 |
| B13 | PD14 | GPIO | I/O | Z | NO PULL | 20 |
| A13 | PD15 | GPIO | I/O | Z | NO PULL | 20 |
| B12 | PD16 | GPIO | I/O | Z | NO PULL | 20 |
| C12 | PD17 | GPIO | I/O | Z | NO PULL | 20 |
| A11 | PD18 | GPIO | I/O | Z | NO PULL | 20 |
| B11 | PD19 | GPIO | I/O | Z | NO PULL | 20 |
| C10 | PD20 | GPIO | I/O | Z | NO PULL | 20 |
| B10 | PD21 | GPIO | I/O | Z | NO PULL | 20 |
| L11,L12 | VCC-PD | POWER | P | - | - | - |
| GPIO E | | | | | | |
| F14 | PE0 | GPIO | I/O | Z | NO PULL | 20 |
| G13 | PE1 | GPIO | I/O | Z | NO PULL | 20 |
| C14 | PE2 | GPIO | I/O | Z | NO PULL | 20 |
| F15 | PE3 | GPIO | I/O | Z | NO PULL | 20 |
| F12 | PE4 | GPIO | I/O | Z | NO PULL | 20 |
| C13 | PE5 | GPIO | I/O | Z | NO PULL | 20 |
| E12 | PE6 | GPIO | I/O | Z | NO PULL | 20 |
| G15 | PE7 | GPIO | I/O | Z | NO PULL | 20 |
| H13 | PE8 | GPIO | I/O | Z | NO PULL | 20 |
| E13 | PE9 | GPIO | I/O | Z | NO PULL | 20 |
| J13 | PE10 | GPIO | I/O | Z | NO PULL | 20 |
| H14 | PE11 | GPIO | I/O | Z | NO PULL | 20 |
| G14 | PE12 | GPIO | I/O | Z | NO PULL | 20 |
| L13 | PE13 | GPIO | I/O | Z | NO PULL | 20 |
| L16 | PE14 | GPIO | I/O | Z | NO PULL | 20 |
| K13 | PE15 | GPIO | I/O | Z | NO PULL | 20 |
| D15 | PE16 | GPIO | I/O | Z | NO PULL | 20 |
| D14 | PE17 | GPIO | I/O | Z | NO PULL | 20 |

| Ball# | Pin Name | Default Function | Type | Reset State | Default Pull Up/Down | Buffer Strength (mA) |
|-----------------------|----------|------------------|------|-------------|----------------------|----------------------|
| E15 | PE18 | GPIO | I/O | Z | NO PULL | 20 |
| E16 | PE19 | GPIO | I/O | Z | NO PULL | 20 |
| H15 | PE20 | GPIO | I/O | Z | NO PULL | 20 |
| G16 | PE21 | GPIO | I/O | Z | NO PULL | 20 |
| J16 | PE22 | GPIO | I/O | Z | NO PULL | 20 |
| L14 | PE23 | GPIO | I/O | Z | NO PULL | 20 |
| K14 | PE24 | GPIO | I/O | Z | NO PULL | 20 |
| M11,M12 | VCC-PE | POWER | P | - | - | - |
| GPIO F | | | | | | |
| R1 | PF0 | GPIO | I/O | JTAG_MS | NO PULL | 20 |
| P1 | PF1 | GPIO | I/O | JTAG_DI | NO PULL | 20 |
| P2 | PF2 | GPIO | I/O | Z | NO PULL | 20 |
| N2 | PF3 | GPIO | I/O | JTAG_DO | NO PULL | 20 |
| N3 | PF4 | GPIO | I/O | Z | NO PULL | 20 |
| M2 | PF5 | GPIO | I/O | JTAG_CK | NO PULL | 20 |
| M1 | PF6 | GPIO | I/O | Z | NO PULL | 20 |
| GPIO G | | | | | | |
| P16 | PG0 | GPIO | I/O | Z | NO PULL | 20 |
| N15 | PG1 | GPIO | I/O | Z | NO PULL | 20 |
| P15 | PG2 | GPIO | I/O | Z | NO PULL | 20 |
| N16 | PG3 | GPIO | I/O | Z | NO PULL | 20 |
| R15 | PG4 | GPIO | I/O | Z | NO PULL | 20 |
| R16 | PG5 | GPIO | I/O | Z | NO PULL | 20 |
| M15 | PG6 | GPIO | I/O | Z | NO PULL | 20 |
| M14 | PG7 | GPIO | I/O | Z | NO PULL | 20 |
| N14 | PG8 | GPIO | I/O | Z | NO PULL | 20 |
| R14 | PG9 | GPIO | I/O | Z | NO PULL | 20 |
| T14 | PG10 | GPIO | I/O | Z | NO PULL | 20 |
| P14 | PG11 | GPIO | I/O | Z | NO PULL | 20 |
| T15 | PG12 | GPIO | I/O | Z | NO PULL | 20 |
| M13 | PG13 | GPIO | I/O | Z | NO PULL | 20 |
| System Control | | | | | | |
| R13 | JTAG_SEL | - | I | - | Pull-Up | - |
| R7 | NMI | - | I | OD | NO PULL | - |
| P7 | RESET | - | I | - | NO PULL | - |
| R4 | X24MIN | - | A | - | - | - |
| P4 | X24MOUT | - | A | - | - | - |
| LRADC | | | | | | |
| T8 | LRADC0 | - | A | - | - | - |
| R8 | LRADC1 | - | A | - | - | - |
| MIPI_CSI | | | | | | |

| Ball# | Pin Name | Default Function | Type | Reset State | Default Pull Up/Down | Buffer Strength (mA) |
|--------------------|---------------|------------------|------|-------------|----------------------|----------------------|
| J1 | MCSI-CKN | - | A | - | - | - |
| J2 | MCSI-CKP | - | A | - | - | - |
| G2 | MCSI-D0N | - | A | - | - | - |
| G3 | MCSI-D0P | - | A | - | - | - |
| H1 | MCSI-D1N | - | A | - | - | - |
| H2 | MCSI-D1P | - | A | - | - | - |
| K1 | MCSI-D2N | - | A | - | - | - |
| K2 | MCSI-D2P | - | A | - | - | - |
| L2 | MCSI-D3N | - | A | - | - | - |
| L3 | MCSI-D3P | - | A | - | - | - |
| M4 | VCC-MCSI | - | A | - | - | - |
| USB | | | | | | |
| R2 | USB-DM | - | A | - | - | - |
| T2 | USB-DP | - | A | - | - | - |
| N7 | VCC-USB | - | P | - | - | - |
| AUDIO_CODEC | | | | | | |
| P8 | AGND | - | G | - | - | - |
| M7 | AVCC | - | P | - | - | - |
| N9 | HBIAS | - | A | - | - | - |
| N12 | HPCOM | - | A | - | - | - |
| N11 | HPCOMFB | - | A | - | - | - |
| P13 | HPOUTL | - | O | - | - | - |
| N13 | HPOUTR | - | O | - | - | - |
| M9 | HPVCCBP | - | A | - | - | - |
| P12 | HPVCCIN | - | P | - | - | - |
| R12 | LINEINL | - | A | - | - | - |
| T12 | LINEINR | - | A | - | - | - |
| R6 | LINEOUTL | - | A | - | - | - |
| T6 | LINEOUTR | - | A | - | - | - |
| P10 | MBIAS | - | A | - | - | - |
| R10 | MICIN1N | - | A | - | - | - |
| T10 | MICIN1P | - | A | - | - | - |
| P11 | MICIN2N | - | A | - | - | - |
| R11 | MICIN2P | - | A | - | - | - |
| R9 | MICIN3N | - | A | - | - | - |
| P9 | MICIN3P | - | A | - | - | - |
| N10 | VRA2 | - | A | - | - | - |
| EPHY | | | | | | |
| K5 | EPHY_LINK_LED | - | A | - | - | - |
| P6 | EPHY_RTX | - | A | - | - | - |
| F1 | EPHY_RXN | - | A | - | - | - |

| Ball# | Pin Name | Default Function | Type | Reset State | Default Pull Up/Down | Buffer Strength (mA) |
|---|--------------|------------------|------|-------------|----------------------|----------------------|
| F2 | EPHY_RXP | - | A | - | - | - |
| L5 | EPHY_SPD_LED | - | A | - | - | - |
| E2 | EPHY_TXN | - | A | - | - | - |
| E3 | EPHY_TXP | - | A | - | - | - |
| M5 | EPHY_VCC | - | P | - | - | - |
| N5 | EPHY_VDD | - | P | - | - | - |
| RTC&PLL | | | | | | |
| T5 | RTC-VIO | - | P | - | - | - |
| T3 | X32KIN | - | A | - | - | - |
| R3 | X32KOUT | - | A | - | - | - |
| P3 | X32KFOUT | - | A | - | - | - |
| N6 | VCC-RTC | - | P | - | - | - |
| L6 | VCC-PLL | - | P | - | - | - |
| DRAM | | | | | | |
| H6 | DVREF | - | P | - | - | - |
| J5 | DZQ | - | AI | - | - | - |
| F6,F7,F8,G8,H8,J8 | VCC-DRAM | - | P | - | - | - |
| Power | | | | | | |
| H11,P5 | VCC-IO | - | P | - | - | - |
| M6 | VDD-EFUSE | - | P | - | - | - |
| G12,H12,J11,J12, K11 | VDD-CPU | - | P | - | - | - |
| K8,K9,L8,M8 | VDD-SYS | - | P | - | - | - |
| A1,A16,C9,D10, D11,D12,D4,D5,D6, D7,D8,D9,E10,E11, E14,E4,E5,E6,E7,E8, E9,F10,F11,F9,G10, G11,G4,G5,G6,G7, G9,H10,H3,H4,H5, H7,H9,J10,J3,J4,J6, J7,J9,K10,K12,K3, K4,K6,K7,L10,L4,L7, L9,M10,N4,N8,R5, T1,T16 | GND | - | G | - | - | - |

Note:

- 1) **Default Function** defines the default function of each pin, especially for pins with multiplexing functions;
- 2) **Type** defines the signal direction: I (Input), O (Output), I/O(Input / Output), OD(Open-Drain),A (Analog), AI(Analog Input),AO(Analog Output),A I/O(Analog Input /Output),P (Power), G (Ground);
- 3) **Reset State** defines the state of the terminal at reset: Z for high-impedance ;
- 4) **Default Pull Up/Down** defines the presence of an internal pull up or pull down resistor. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down;
- 5) **Buffer Strength** defines drive strength of the associated output buffer.

3.2. GPIO Multiplexing Functions

The following table provides a description of the S3 GPIO multiplexing functions.

Table 3-2. Multiplexing Functions

| Pin Name | Default Function | IO Type | Default IO State | Default Pull-up/down | Function 2 | Function3 | Function 4 | Function 5 | Function 6 |
|----------|------------------|---------|------------------|----------------------|------------|-----------|--|------------|------------|
| PB0 | GPIO | I/O | DIS | Z | UART2_TX | - | - | - | PB_EINT0 |
| PB1 | | I/O | DIS | Z | UART2_RX | - | - | - | PB_EINT1 |
| PB2 | | I/O | DIS | Z | UART2_RTS | - | - | - | PB_EINT2 |
| PB3 | | I/O | DIS | Z | UART2_CTS | - | - | - | PB_EINT3 |
| PB4 | | I/O | DIS | Z | PWM0 | - | - | - | PB_EINT4 |
| PB5 | | I/O | DIS | Z | PWM1 | - | - | - | PB_EINT5 |
| PB6 | | I/O | DIS | Z | TWI0_SCK | - | - | - | PB_EINT6 |
| PB7 | | I/O | DIS | Z | TWI0_SDA | - | - | - | PB_EINT7 |
| PB8 | | I/O | DIS | Z | TWI1_SCK | UART0_TX | - | - | PB_EINT8 |
| PB9 | | I/O | DIS | Z | TWI1_SDA | UART0_RX | - | - | PB_EINT9 |
| PB10 | | I/O | DIS | Z | JTAG_MS | - | - | - | PB_EINT10 |
| PB11 | | I/O | DIS | Z | JTAG_CK | - | - | - | PB_EINT11 |
| PB12 | | I/O | DIS | Z | JTAG_DO | - | - | - | PB_EINT12 |
| PB13 | | I/O | DIS | Z | JTAG_DI | - | - | - | PB_EINT13 |
| PC0 | GPIO | I/O | DIS | Z | SDC2_CLK | SPI0_MISO | - | - | - |
| PC1 | | I/O | DIS | Z | SDC2_CMD | SPI0_CLK | - | - | - |
| PC2 | | I/O | DIS | Z | SDC2_RST | SPI0_CS | - | - | - |
| PC3 | | I/O | DIS | Z | SDC2_D0 | SPI0_MOSI | - | - | - |
| PC4 | | I/O | DIS | Z | SDC2_D1 | - | - | - | - |
| PC5 | | I/O | DIS | Z | SDC2_D2 | - | - | - | - |
| PC6 | | I/O | DIS | Z | SDC2_D3 | - | - | - | - |
| PC7 | | I/O | DIS | Z | SDC2_D4 | - | - | - | - |
| PC8 | | I/O | DIS | Z | SDC2_D5 | - | - | - | - |
| PC9 | | I/O | DIS | Z | SDC2_D6 | - | - | - | - |
| PC10 | | I/O | DIS | Z | SDC2_D7 | - | - | - | - |
| PD0 | GPIO | I/O | DIS | Z | LCD_D2 | - | RGMII_RXD3/ MII_RXD3 / RMII_NULL | - | - |
| PD1 | | I/O | DIS | Z | LCD_D3 | - | RGMII_RXD2/ MII_RXD2/ RMII_NULL | - | - |
| PD2 | | I/O | DIS | Z | LCD_D4 | - | RGMII_RXD1/ MII_RXD1/ RMII_RXD1 | - | - |
| PD3 | | I/O | DIS | Z | LCD_D5 | - | RGMII_RXD0/ MII_RXD0/ RMII_RXD0 | - | - |
| PD4 | | I/O | DIS | Z | LCD_D6 | - | RGMII_RXCK/ MII_RXCK/ RMII_NULL | - | - |
| PD5 | | I/O | DIS | Z | LCD_D7 | - | RGMII_RXCTL/ MII_RXDV/ | - | - |

| Pin Name | Default Function | IO Type | Default IO State | Default Pull-up/down | Function 2 | Function3 | Function 4 | Function 5 | Function 6 |
|----------|------------------|---------|------------------|----------------------|------------|-----------|--|------------|------------|
| | | | | | | | RMII_CRD_DV | | |
| PD6 | | I/O | DIS | Z | LCD_D10 | - | RGMII_NULL/ MII_RXERR/ RMII_RXER | - | - |
| PD7 | | I/O | DIS | Z | LCD_D11 | - | RGMII_TXD3/ MII_TXD3/ RMII_NULL | - | - |
| PD8 | | I/O | DIS | Z | LCD_D12 | - | RGMII_TXD2/ MII_TXD2/ RMII_NULL | - | - |
| PD9 | | I/O | DIS | Z | LCD_D13 | - | RGMII_TXD1/ MII_TXD1/ RMII_TXD1 | - | - |
| PD10 | | I/O | DIS | Z | LCD_D14 | - | RGMII_TXD0/ MII_TXD0/ RMII_TXD0 | - | - |
| PD11 | | I/O | DIS | Z | LCD_D15 | - | RGMII_NULL/ MII_CRD/ RMII_NULL | - | - |
| PD12 | | I/O | DIS | Z | LCD_D18 | LVDS_VP0 | RGMII_TXCK/ MII_TXCK/ RMII_TXCK | - | - |
| PD13 | | I/O | DIS | Z | LCD_D19 | LVDS_VN0 | RGMII_TXCTL/ MII_TXEN/ RMII_TXEN | - | - |
| PD14 | | I/O | DIS | Z | LCD_D20 | LVDS_VP1 | RGMII_NULL/ MII_TXERR/ RMII_NULL | - | - |
| PD15 | | I/O | DIS | Z | LCD_D21 | LVDS_VN1 | RGMII_CLKIN/ MII_COL/ RMII_NULL | - | - |
| PD16 | | I/O | DIS | Z | LCD_D22 | LVDS_VP2 | MDC | - | - |
| PD17 | | I/O | DIS | Z | LCD_D23 | LVDS_VN2 | MDIO | - | - |
| PD18 | | I/O | DIS | Z | LCD_CLK | LVDS_VPC | - | - | - |
| PD19 | | I/O | DIS | Z | LCD_DE | LVDS_VNC | - | - | - |
| PD20 | | I/O | DIS | Z | LCD_HSYNC | LVDS_VP3 | - | - | - |
| PD21 | | I/O | DIS | Z | LCD_VSYNC | LVDS_VN3 | - | - | - |
| PE0 | GPIO | I/O | DIS | Z | CSI_PCLK | LCD_CLK | - | - | - |
| PE1 | | I/O | DIS | Z | CSI_MCLK | LCD_DE | - | - | - |
| PE2 | | I/O | DIS | Z | CSI_HSYNC | LCD_HSYNC | - | - | - |
| PE3 | | I/O | DIS | Z | CSI_VSYNC | LCD_VSYNC | - | - | - |
| PE4 | | I/O | DIS | Z | CSI_D0 | LCD_D2 | - | - | - |
| PE5 | | I/O | DIS | Z | CSI_D1 | LCD_D3 | - | - | - |
| PE6 | | I/O | DIS | Z | CSI_D2 | LCD_D4 | - | - | - |
| PE7 | | I/O | DIS | Z | CSI_D3 | LCD_D5 | - | - | - |
| PE8 | | I/O | DIS | Z | CSI_D4 | LCD_D6 | - | - | - |
| PE9 | | I/O | DIS | Z | CSI_D5 | LCD_D7 | - | - | - |
| PE10 | | I/O | DIS | Z | CSI_D6 | LCD_D10 | - | - | - |
| PE11 | | I/O | DIS | Z | CSI_D7 | LCD_D11 | - | - | - |
| PE12 | I/O | DIS | Z | CSI_D8 | LCD_D12 | - | - | - | |

| Pin Name | Default Function | IO Type | Default IO State | Default Pull-up/down | Function 2 | Function3 | Function 4 | Function 5 | Function 6 |
|----------|------------------|---------|------------------|----------------------|------------|----------------|------------|------------|------------|
| PE13 | | I/O | DIS | Z | CSI_D9 | LCD_D13 | - | - | - |
| PE14 | | I/O | DIS | Z | CSI_D10 | LCD_D14 | - | - | - |
| PE15 | | I/O | DIS | Z | CSI_D11 | LCD_D15 | - | - | - |
| PE16 | | I/O | DIS | Z | CSI_D12 | LCD_D18 | - | - | - |
| PE17 | | I/O | DIS | Z | CSI_D13 | LCD_D19 | - | - | - |
| PE18 | | I/O | DIS | Z | CSI_D14 | LCD_D20 | - | - | - |
| PE19 | | I/O | DIS | Z | CSI_D15 | LCD_D21 | - | - | - |
| PE20 | | I/O | DIS | Z | CSI_FIELD | CSI_MIPI_M CLK | - | - | - |
| PE21 | | I/O | DIS | Z | CSI_SCK | TWI1_SCK | UART1_TX | - | - |
| PE22 | | I/O | DIS | Z | CSI_SDA | TWI1_SDA | UART1_RX | - | - |
| PE23 | | I/O | DIS | Z | - | LCD_D22 | UART1_RTS | - | - |
| PE24 | | I/O | DIS | Z | - | LCD_D23 | UART1_CTS | - | - |
| PF0 | | GPIO | I/O | JTAG_MS | Z | SDC0_D1 | JTAG_MS | - | - |
| PF1 | I/O | | JTAG_DI | Z | SDC0_D0 | JTAG_DI | - | - | - |
| PF2 | I/O | | DIS | Z | SDC0_CLK | UART0_TX | - | - | - |
| PF3 | I/O | | JTAG_DO | Z | SDC0_CMD | JTAG_DO | - | - | - |
| PF4 | I/O | | DIS | Z | SDC0_D3 | UART0_RX | - | - | - |
| PF5 | I/O | | JTAG_CK | Z | SDC0_D2 | JTAG_CK | - | - | - |
| PF6 | I/O | | DIS | Z | | | - | - | - |
| PG0 | GPIO | I/O | DIS | Z | SDC1_CLK | - | - | - | PG_EINT0 |
| PG1 | | I/O | DIS | Z | SDC1_CMD | - | - | - | PG_EINT1 |
| PG2 | | I/O | DIS | Z | SDC1_D0 | - | - | - | PG_EINT2 |
| PG3 | | I/O | DIS | Z | SDC1_D1 | - | - | - | PG_EINT3 |
| PG4 | | I/O | DIS | Z | SDC1_D2 | - | - | - | PG_EINT4 |
| PG5 | | I/O | DIS | Z | SDC1_D3 | - | - | - | PG_EINT5 |
| PG6 | | I/O | DIS | Z | UART1_TX | - | - | - | PG_EINT6 |
| PG7 | | I/O | DIS | Z | UART1_RX | - | - | - | PG_EINT7 |
| PG8 | | I/O | DIS | Z | UART1_RTS | - | - | - | PG_EINT8 |
| PG9 | | I/O | DIS | Z | UART1_CTS | - | - | - | PG_EINT9 |
| PG10 | | I/O | DIS | Z | PCM_SYNC | - | - | - | PG_EINT10 |
| PG11 | | I/O | DIS | Z | PCM_BCLK | - | - | - | PG_EINT11 |
| PG12 | | I/O | DIS | Z | PCM_DOUT | - | - | - | PG_EINT12 |
| PG13 | I/O | DIS | Z | PCM_DIN | - | - | - | PG_EINT13 | |

3.3. Detailed Pin/Signal Description

The following table shows the detailed function description of every pin/signal based on the different interface.

Table 3-3. Detailed Pin Description

| Pin/Signal Name | Description | Type |
|-----------------------|--|-------|
| DRAM | | |
| DZQ | DRAM ZQ Calibration | AI |
| DVREF | DRAM Reference Voltage Input | P |
| VCC-DRAM | DRAM Power Supply | P |
| System Control | | |
| NMI | Non-Maskable Interrupt | I |
| RESET | RESET Signal | I |
| JTAG_SEL | JTAG Mode Select | I |
| X24MIN | Clock Input of 24MHz Crystal | AI |
| X24MOUT | Clock Output of 24MHz Crystal | AO |
| RTC&PLL | | |
| RTC-VIO | Internal LDO Output Bypass | P |
| X32KIN | Clock Input of 32768Hz Crystal | AI |
| X32KOUT | Clock Output of 32768Hz Crystal | AO |
| X32KFOUT | Clock Output of LOSC | OD |
| VCC-RTC | RTC Power Supply | P |
| VCC-PLL | PLL Power Supply | P |
| USB | | |
| USB-DM | USB Data Signal Negative | A I/O |
| USB-DP | USB Data Signal Positive | A I/O |
| VCC-USB | USB Power Supply | P |
| LRADC | | |
| LRADC0 | ADC Input for Key0 | AI |
| LRADC1 | ADC Input for Key1 | AI |
| AUDIO CODEC | | |
| LINEINL | LINE-IN Left Channel Input | AI |
| LINEINR | LINE-IN Right Channel Input | AI |
| LINEOUTL | LINE-OUT Left Channel Output | AO |
| LINEOUTR | LINE-OUT Right Channel Output | AO |
| HBIAS | Master Analog Headphone Bias Voltage Output | AO |
| HPCOM | Headphone Common Reference Output | AO |
| HPCOMFB | Headphone Common Reference Feedback Input | AI |
| HPOUTL | Headphone Output Left Channel | AO |
| HPOUTR | Headphone Output Right Channel | AO |
| HPVCCBP | Headphone VCC Bypass | AO |
| HPVCCIN | Headphone VCC Input | P |
| MBIAS | Master Analog Microphone Bias Voltage Output | AO |

| Pin/Signal Name | Description | Type |
|------------------|--|-------|
| MICIN1N | Microphone Negative Input 1 | AI |
| MICIN1P | Microphone Positive Input 1 | AI |
| MICIN2N | Microphone Negative Input2 | AI |
| MICIN2P | Microphone Positive Input 2 | AI |
| MICIN3N | Microphone Negative Input 3 | AI |
| MICIN3P | Microphone Positive Input 3 | AI |
| VRA2 | Reference Voltage | AO |
| AVCC | Power Supply for Analog Part | P |
| EPHY | | |
| EPHY_RXP | Transceiver Positive Output/Input | A I/O |
| EPHY_RXN | Transceiver Negative Output/Input | A I/O |
| EPHY_TXP | Transceiver Positive Output/Input | A I/O |
| EPHY_TXN | Transceiver Negative Output/Input | A I/O |
| EPHY_RTX | EPHY External Resistance to Ground | AI |
| EPHY_LINK_LED | EPHY LINK Up/Down Indicator LED | O |
| EPHY_SPD_LED | EPHY 10M/100M Indicator LED | O |
| EPHY_VDD | Analog Low Power Supply for EPHY | P |
| EPHY_VCC | Analog High Power Supply for EPHY | P |
| SD /MMC | | |
| SDC0_CMD | Command Signal for SD/TF Card | I/O |
| SDC0_CLK | Clock for SD/TF Card | O |
| SDC0_D[3:0] | Data Input and Output for SD/TF Card | I/O |
| SDC1_CMD | Command Signal for SDIO WIFI | I/O |
| SDC1_CLK | Clock for SDIO WIFI | O |
| SDC1_D[3:0] | Data Input and Output for SDIO WIFI | I/O |
| SDC2_CMD | Command Signal for SD/eMMC | I/O |
| SDC2_CLK | Clock for SD/eMMC | O |
| SDC2_D[7:0] | Data Input and Output for SD/eMMC | I/O |
| SDC2_RST | Reset Signal for SD/eMMC | O |
| I2S/PCM | | |
| PCM_SYNC | I2S/PCM Sample Rate Clock/Sync | I/O |
| PCM_BCLK | I2S/PCM Sample Rate Clock | I/O |
| PCM_DOUT | I2S/PCM Serial Data Output | O |
| PCM_DIN | I2S/PCM Serial Data Input | I |
| Interrupt | | |
| PB_EINT[21:0] | GPIO B Interrupt | I |
| PG_EINT[13:0] | GPIO G Interrupt | I |
| PWM | | |
| PWM0 | Pulse Width Modulation Output Channel0 | O |
| PWM1 | Pulse Width Modulation Output Channel1 | O |
| LCD | | |
| LCD_D[23:0] | LCD Data Output | O |

| Pin/Signal Name | Description | Type |
|---------------------------------|--|------|
| LCD_CLK | LCD Clock Signal | O |
| LCD_DE | LCD Data Enable | O |
| LCD_HSYNC | LCD Horizontal SYNC | O |
| LCD_VSYNC | LCD Vertical SYNC | O |
| LVDS | | |
| LVDS_VP[3:0] | LVDS Data Positive Signal Output | AO |
| LVDS_VN[3:0] | LVDS Data Negative Signal Output | AO |
| LVDS_VPC | LVDS Clock Positive Signal Output | AO |
| LVDS_VNC | LVDS Clock Negative Signal Output | AO |
| CSI | | |
| CSI_PCLK | CSI Pixel Clock | I |
| CSI_MCLK | CSI Master Clock | O |
| CSI_HSYNC | CSI Horizontal SYNC | I |
| CSI_VSYNC | CSI Vertical SYNC | I |
| CSI_D[15:0] | CSI Data Input | I |
| CSI_SCK | CSI Command Serial Clock Signal | I/O |
| CSI_SDA | CSI Command Serial Data Signal | I/O |
| CSI_FIELD | CSI Field Signal | I/O |
| MIPI_CSI | | |
| MCSI-CKN | MIPI CSI Negative Differential Clock Line | AI |
| MCSI-CKP | MIPI CSI Positive Differential Clock Line | AI |
| MCSI-D0N | MIPI CSI Negative Differential Data Line0 | AI |
| MCSI-D0P | MIPI CSI Positive Differential Data Line0 | AI |
| MCSI-D1N | MIPI CSI Negative Differential Data Line1 | AI |
| MCSI-D1P | MIPI CSI Positive Differential Data Line1 | AI |
| MCSI-D2N | MIPI CSI Negative Differential Data Line2 | AI |
| MCSI-D2P | MIPI CSI Positive Differential Data Line2 | AI |
| MCSI-D3N | MIPI CSI Negative Differential Data Line3 | AI |
| MCSI-D3P | MIPI CSI Positive Differential Data Line3 | AI |
| VCC-MCSI | MIPI CSI Power Supply | P |
| EMAC | | |
| RGMII_RXD3/MII_RXD3/RMII_NULL | RGMII/MII Receive Data | I |
| RGMII_RXD2/MII_RXD2/RMII_NULL | RGMII/MII Receive Data | I |
| RGMII_RXD1/MII_RXD1/RMII_RXD1 | RGMII/MII /RMII Receive Data | I |
| RGMII_RXD0/MII_RXD0/RMII_RXD0 | RGMII/MII /RMII Receive Data | I |
| RGMII_RXCK/MII_RXCK/RMII_NULL | RGMII/MII Receive Clock | I |
| RGMII_RXCTL/MII_RXDV/RMII_CRSDV | RGMII Receive Control/MII Receive Enable/RMII Carrier Sense-Receive Data Valid | I |
| RGMII_NULL/MII_RXERR/RMII_RXER | MII/RMII Receive Error | I |
| RGMII_TXD3/MII_TXD3/RMII_NULL | RGMII/MII Transmit Data | O |
| RGMII_TXD2/MII_TXD2/RMII_NULL | RGMII/MII Transmit Data | O |
| RGMII_TXD1/MII_TXD1/RMII_TXD1 | RGMII/MII /RMII Transmit Data | O |

| Pin/Signal Name | Description | Type |
|--------------------------------|---|------|
| RGMII_TXD0/MII_TXD0/ RMII_TXD0 | RGMII/MII /RMII Transmit Data | O |
| RGMII_NULL/MII_CRD/RMII_NULL | MII Carrier Sense | I |
| RGMII_TXCK/MII_TXCK/RMII_TXCK | RGMII/MII /RMII Transmit Clock: Output Pin for RGMII, Input Pin for MII/RMII | I/O |
| RGMII_TXCTL/MII_TXEN/RMII_TXEN | RGMII Transmit Control/MII Transmit Enable/RMII Transmit Enable: Output Pin for RGMII/RMII, Input Pin for MII | I/O |
| RGMII_NULL/MII_TXERR/RMII_NULL | MII Transmit Error | O |
| RGMII_CLKIN/MII_COL/RMII_NULL | RGMII Transmit Clock from External/MII Collision Detect | I |
| MDC | RGMII/MII /RMII Management Data Clock | O |
| MDIO | RGMII/MII /RMII Management Data Input/Output | I/O |
| SPI | | |
| SPI0_CS | SPI Chip Select signal, Low Active | I/O |
| SPI0_CLK | SPI Clock Signal | I/O |
| SPI0_MOSI | SPI Master Data Out, Slave Data In | I/O |
| SPI0_MISO | SPI Master Data In, Slave Data Out | I/O |
| UART | | |
| UART0_TX | UART0 Data Transmit | O |
| UART0_RX | UART0 Data Receive | I |
| UART1_TX | UART1 Data Transmit | O |
| UART1_RX | UART1 Data Receive | I |
| UART1_CTS | UART1 Data Clear To Send | I |
| UART1_RTS | UART1 Data Request To Send | O |
| UART2_TX | UART2 Data Transmit | O |
| UART2_RX | UART2 Data Receive | I |
| UART2_CTS | UART2 Data Clear To Send | I |
| UART2_RTS | UART2 Data Request To Send | O |
| TWI | | |
| TWI0_SCK | TWI0 Serial Clock Signal | I/O |
| TWI0_SDA | TWI0 Serial Data Signal | I/O |
| TWI1_SCK | TWI1 Serial Clock Signal | I/O |
| TWI1_SDA | TWI1 Serial Data Signal | I/O |
| JTAG | | |
| JTAG_MS | JTAG Mode Select | I |
| JTAG_CK | JTAG Clock Signal | I |
| JTAG_DO | JTAG Data Output | O |
| JTAG_DI | JTAG Data Input | I |

Chapter 4 System

This section describes the S3 system part from the following aspects:

- Boot System
- CCU
- System Control
- Timer
- High-speed Timer
- PWM
- DMA
- GIC
- Crypto Engine
- Security ID
- LRADC
- RTC
- Audio Codec
- Port Controller

Sochip

4.1. Memory Mapping

| Module | Address | Size (byte) |
|---------------------|--|-------------|
| SRAM A1 | 0x0000 0000---0x0000 3FFF | 16K |
| SRAM C | 0x0000 4000---0x0000 EFFF | 44K |
| DE | 0x0100 0000---0x011F FFFF | 2M |
| System Control | 0x01C0 0000---0x01C0 0FFF | 4K |
| DMA | 0x01C0 2000---0x01C0 2FFF | 4K |
| TCON | 0x01C0 C000---0x01C0 CFFF | 4K |
| VE | 0x01C0 E000---0x01C0 EFFF | 4K |
| SD/MMC 0 | 0x01C0 F000---0x01C0 FFFF | 4K |
| SD/MMC 1 | 0x01C1 0000---0x01C1 0FFF | 4K |
| SD/MMC 2 | 0x01C1 1000---0x01C1 1FFF | 4K |
| SID | 0x01C1 4000---0x01C1 43FF | 1K |
| Crypto Engine | 0x01C1 5000---0x01C1 5FFF | 4K |
| USB OTG_Device | 0x01C1 9000---0x01C1 9FFF | 4K |
| USB OTG_EHCI0/OHCI0 | 0x01C1 A000---0x01C1 AFFF | 4K |
| CCU | 0x01C2 0000---0x01C2 03FF | 1K |
| PIO | 0x01C2 0800---0x01C2 0BFF | 1K |
| TIMER | 0x01C2 0C00---0x01C2 0FFF | 1K |
| PWM | 0x01C2 1400---0x01C2 17FF | 1K |
| I2S/PCM | 0x01C2 2000---0x01C2 23FF | 1K |
| LRADC | 0x01C2 2800---0x01C2 2BFF | 1K |
| AC | 0x01C2 2C00---0x01C2 33FF | 2K |
| UART 0 | 0x01C2 8000---0x01C2 83FF | 1K |
| UART 1 | 0x01C2 8400---0x01C2 87FF | 1K |
| UART 2 | 0x01C2 8800---0x01C2 8BFF | 1K |
| TWI 0 | 0x01C2 AC00---0x01C2 AFFF | 1K |
| TWI 1 | 0x01C2 B000---0x01C2 B3FF | 1K |
| EMAC | 0x01C3 0000---0x01C3 FFFF | 64K |
| HSTMR | 0x01C6 0000---0x01C6 0FFF | 4K |
| DRAMCOM | 0x01C6 2000---0x01C6 2FFF | 4K |
| DRAMCTL0 | 0x01C6 3000---0x01C6 3FFF | 4K |
| DRAMPHY0 | 0x01C6 5000---0x01C6 5FFF | 4K |
| SPI | 0x01C6 8000---0x01C6 8FFF | 4K |
| SCU Space | 0x01C80000 GIC_DIST: 0x01C80000 + 0x1000 GIC_CPUIF:0x01C80000 + 0x2000 | |
| CSI | 0x01CB 0000---0x01CF FFFF | 320K |
| RTC | 0x01c2 0400---0x01C2 07FF | 1K |
| CoreSight Debug | 0x3F50 0000---0x3F51 FFFF | 128K |
| TSGEN RO | 0x3F50 6000---0x3F50 6FFF | 4K |
| TSGEN CTRL | 0x3F50 7000---0x3F50 7FFF | 4K |
| DRAM | 0x4000 0000---0xBFFF FFFF | 2G |
| BROM | 0xFFFF 0000---0xFFFF 7FFF | 32K |

4.2. Boot System

The boot system can boot from SPI NOR Flash,SPI NAND Flash,SD Card and USB for different application. There is one 32KB ROM In the system .The SPI0,SDC0,SDC2 controller are used for booting system.

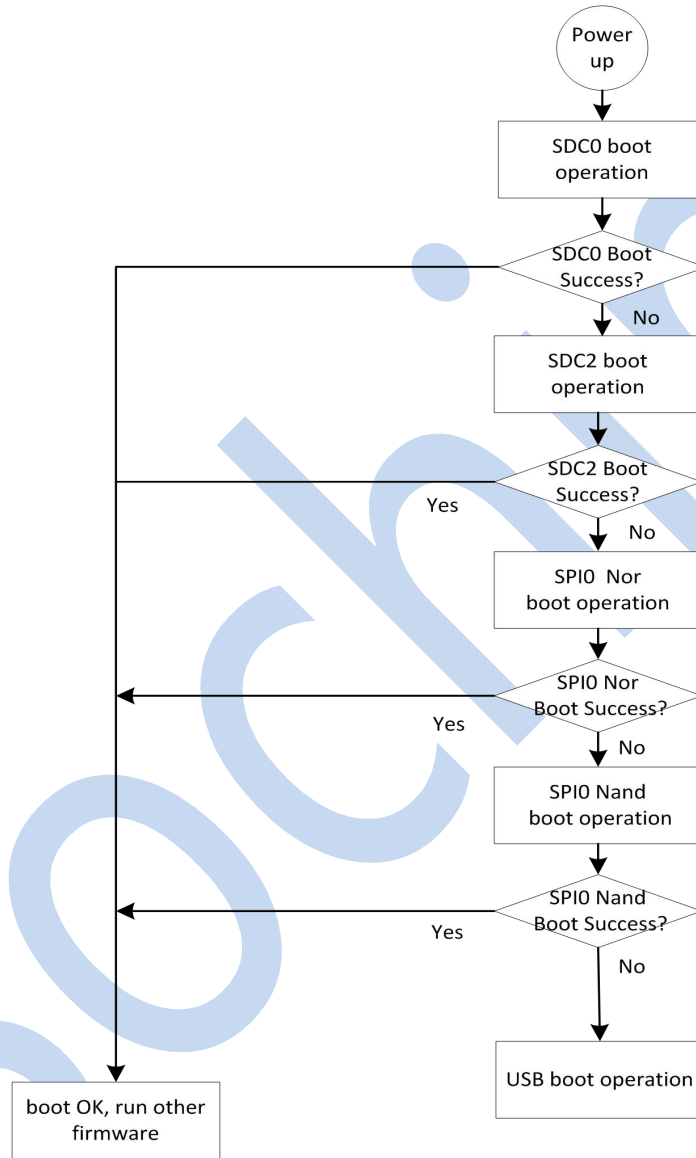


Figure 4-1. Boot System Sequence Diagram

4.3. CCU

4.3.1. Overview

The CCU controls the PLLs configuration and most of the clock generation, division, distribution, synchronization and gating. CCU input signals include the external clock for the reference frequency (24MHz). The outputs from CCU are mostly clocks to other blocks in the system.

The CCU includes the following features:

- 9 PLLs, independent PLL for CPU
- Bus Source and Divisions
- Clock Output Control
- PLLs Bias Control
- PLLs Tuning Control
- PLLs Pattern Control
- Configuring Modules Clock
- Bus Clock Gating
- Bus Software Reset

4.3.2. Functionalities Description

4.3.2.1. System Bus

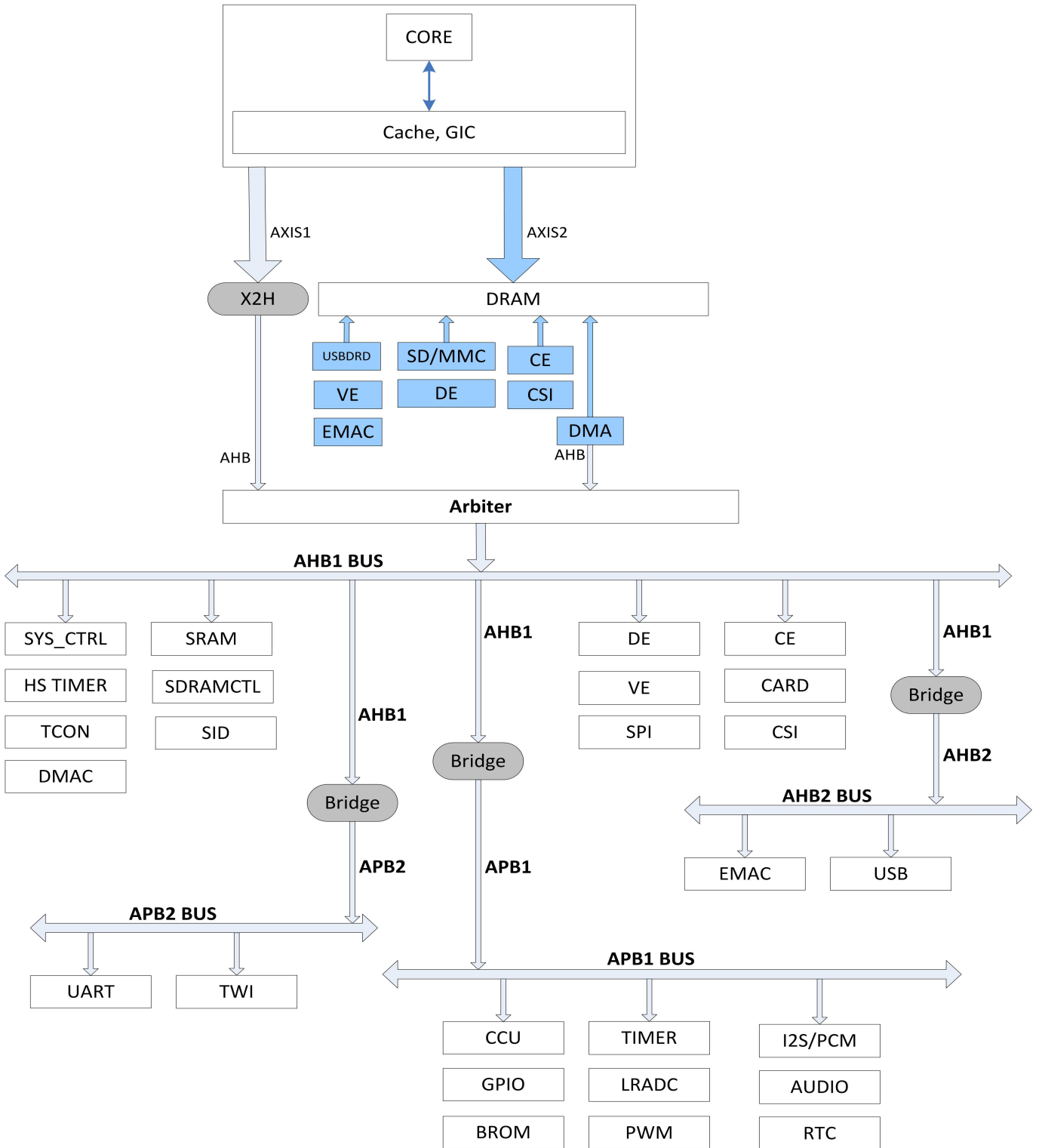


Figure 4-2. System Bus Tree

4.3.2.2. Bus Clock Tree

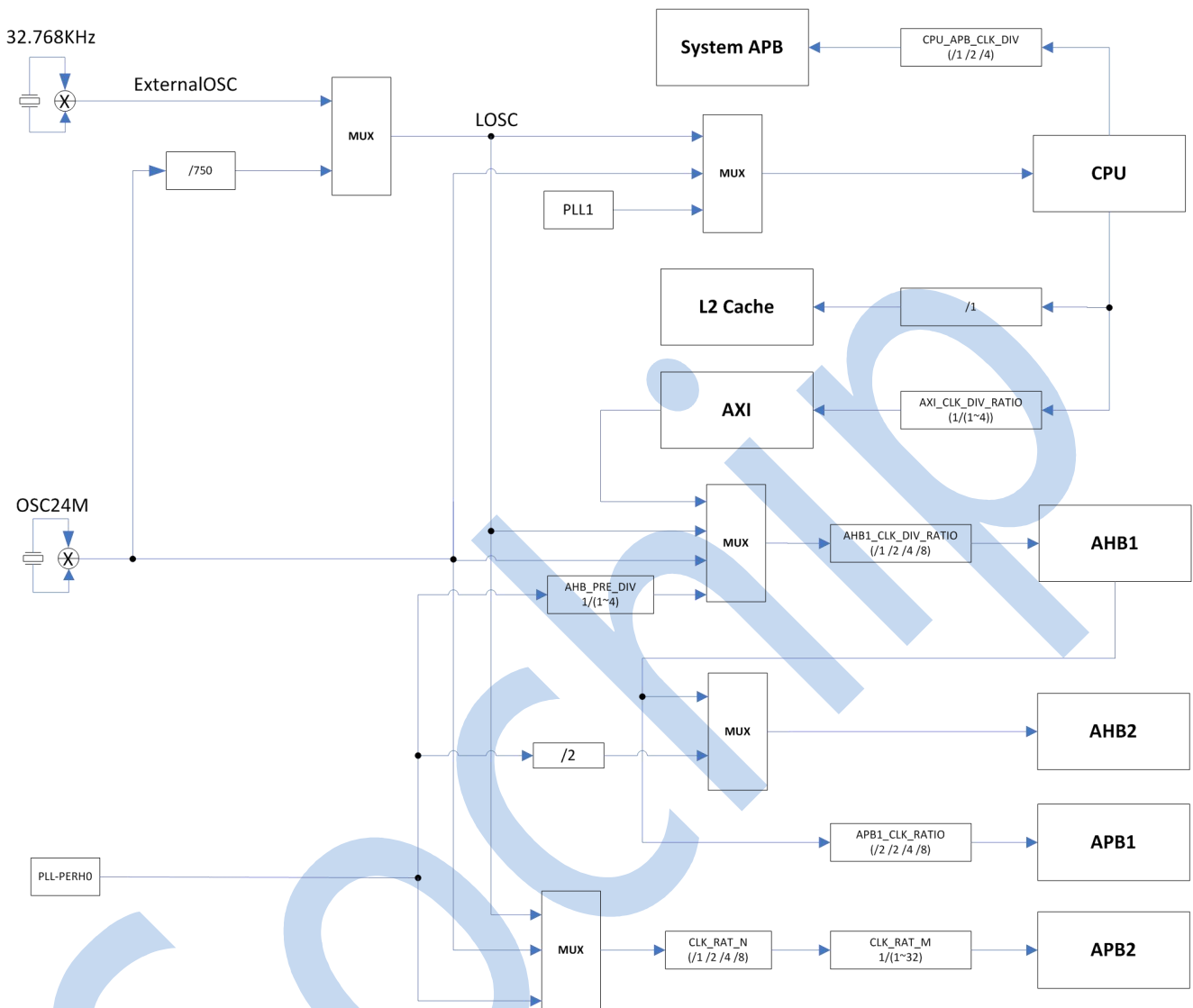


Figure 4-3. Bus Clock Tree

4.3.3. Typical Applications

- Clock output of PLL_CPU is used only for CPU, and the frequency factor can be dynamically modified for DVFS;
- Clock output of PLL_AUDIO can be used for I2S/PCM, AC DIGITAL etc, and dynamic frequency scaling is not supported;
- Clock output of PLL_PERIPH0 can be used for MBUS/AHB1/APB1/APB2 and MMC0/MMC1/MMC2//CE/SPI/DE etc, and dynamic frequency scaling is not supported;
- Clock output of PLL_PERIPH1 can be used for MMC0/MMC1/MMC2/SPI etc, and dynamic frequency scaling is not supported;
- Clock output of PLL_VIDEO can be used for DE/TCON/CSI, and dynamic frequency scaling is not supported;
- Clock output of PLL_VE can be used for CSI/VE, and dynamic frequency scaling is not supported;
- Clock output of PLL_DDR0 can be used for MBUS and DRAM, and dynamic frequency scaling is not supported;
- Clock output of PLL_DDR1 can be used for DRAM, and dynamic frequency scaling is supported;

4.3.4. Register List

| Module Name | Base Address |
|-------------|--------------|
| CCU | 0x01C20000 |

| Register Name | Offset | Description |
|----------------------|--------|---------------------------------|
| PLL_CPU_CTRL_REG | 0x0000 | PLL_CPU Control Register |
| PLL_AUDIO_CTRL_REG | 0x0008 | PLL_AUDIO Control Register |
| PLL_VIDEO_CTRL_REG | 0x0010 | PLL_VIDEO Control Register |
| PLL_VE_CTRL_REG | 0x0018 | PLL_VE Control Register |
| PLL_DDR0_CTRL_REG | 0x0020 | PLL_DDR0 Control Register |
| PLL_PERIPHO_CTRL_REG | 0x0028 | PLL_PERIPHO Control Register |
| PLL_ISP_CTRL_REG | 0x002C | PLL_ISP Control Register |
| PLL_PERIPH1_CTRL_REG | 0x0044 | PLL_PERIPH1 Control Register |
| PLL_DDR1_CTRL_REG | 0x004C | PLL_DDR1 Control Register |
| CPU_AXI_CFG_REG | 0x0050 | CPU/AXI Configuration Register |
| AHB_APB0_CFG_REG | 0x0054 | AHB/APB0 Configuration Register |
| APB1_CFG_REG | 0x0058 | APB1 Configuration Register |
| AHB2_CFG_REG | 0x005C | AHB2 Configuration Register |
| BUS_CLK_GATING_REG0 | 0x0060 | Bus Clock Gating Register 0 |
| BUS_CLK_GATING_REG1 | 0x0064 | Bus Clock Gating Register 1 |
| BUS_CLK_GATING_REG2 | 0x0068 | Bus Clock Gating Register 2 |
| BUS_CLK_GATING_REG3 | 0x006C | Bus Clock Gating Register 3 |
| BUS_CLK_GATING_REG4 | 0x0070 | Bus Clock Gating Register4 |
| SDMMC0_CLK_REG | 0x0088 | SDMMC0 Clock Register |
| SDMMC1_CLK_REG | 0x008C | SDMMC1 Clock Register |
| SDMMC2_CLK_REG | 0x0090 | SDMMC2 Clock Register |
| CE_CLK_REG | 0x009C | CE Clock Register |
| SPI_CLK_REG | 0x00A0 | SPI Clock Register |
| I2S/PCM_CLK_REG | 0x00B0 | I2S/PCM Clock Register |
| USBPHY_CFG_REG | 0x00CC | USBPHY Configuration Register |
| DRAM_CFG_REG | 0x00F4 | DRAM Configuration Register |
| PLL_DDR1_CFG_REG | 0x00F8 | PLL_DDR Configuration Register |
| MBUS_RST_REG | 0x00FC | MBUS Reset Register |
| DRAM_CLK_GATING_REG | 0x0100 | DRAM Clock Gating Register |
| DE_CLK_REG | 0x0104 | DE Clock Register |
| TCON_CLK_REG | 0x0118 | TCON Clock Register |
| CSI_MISC_CLK_REG | 0x0130 | CSI_MISC Clock Register |
| CSI_CLK_REG | 0x0134 | CSI Clock Register |
| VE_CLK_REG | 0x013C | VE Clock Register |
| AC_DIG_CLK_REG | 0x0140 | AC Digital Clock Register |
| AVS_CLK_REG | 0x0144 | AVS Clock Register |
| MBUS_CLK_REG | 0x015C | MBUS Clock Register |
| MIPI_CSI_REG | 0x016C | MIPI_CSI Register |
| PLL_STABLE_TIME_REG0 | 0x0200 | PLL Stable Time Register0 |
| PLL_STABLE_TIME_REG1 | 0x0204 | PLL Stable Time Register1 |
| PLL_CPU_BIAS_REG | 0x0220 | PLL_CPU Bias Register |
| PLL_AUDIO_BIAS_REG | 0x0224 | PLL_AUDIO Bias Register |
| PLL_VIDEO_BIAS_REG | 0x0228 | PLL_VIDEO Bias Register |
| PLL_VE_BIAS_REG | 0x022C | PLL_VE Bias Register |
| PLL_DDR0_BIAS_REG | 0x0230 | PLL_DDR0 Bias Register |
| PLL_PERIPHO_BIAS_REG | 0x0234 | PLL_PERIPHO Bias Register |
| PLL_ISP_BIAS_REG | 0x0238 | PLL_ISP Bias Register |

| | | |
|--------------------------|--------|--------------------------------------|
| PLL_PERIPH1_BIAS_REG | 0x0244 | PLL_PERIPH1 Bias Register |
| PLL_DDR1_BIAS_REG | 0x024C | PLL_DDR1 Bias Register |
| PLL_CPU_TUN_REG | 0x0250 | PLL_CPU Tuning Register |
| PLL_DDR0_TUN_REG | 0x0260 | PLL_DDR0 Tuning Register |
| PLL_CPU_PAT_CTRL_REG | 0x0280 | PLL_CPU Pattern Control Register |
| PLL_AUDIO_PAT_CTRL_REG | 0x0284 | PLL_AUDIO Pattern Control Register |
| PLL_VIDEO_PAT_CTRL_REG | 0x0288 | PLL_VIDEO Pattern Control Register |
| PLL_VE_PAT_CTRL_REG | 0x028C | PLL_VE Pattern Control Register |
| PLL_DDR0_PAT_CTRL_REG | 0x0290 | PLL_DDR0 Pattern Control Register |
| PLL_ISP_PAT_CTRL_REG | 0x0298 | PLL_ISP Pattern Control Register |
| PLL_PERIPH1_PAT_CTRL_REG | 0x02A4 | PLL_PERIPH1 Pattern Control Register |
| PLL_DDR1_PAT_CTRL_REG0 | 0x02AC | PLL_DDR1 Pattern Control Register0 |
| PLL_DDR1_PAT_CTRL_REG1 | 0x02B0 | PLL_DDR1 Pattern Control Register1 |
| BUS_SOFT_RST_REG0 | 0x02C0 | Bus Software Reset Register 0 |
| BUS_SOFT_RST_REG1 | 0x02C4 | Bus Software Reset Register 1 |
| BUS_SOFT_RST_REG2 | 0x02C8 | Bus Software Reset Register 2 |
| BUS_SOFT_RST_REG3 | 0x02D0 | Bus Software Reset Register 3 |
| BUS_SOFT_RST_REG4 | 0x02D8 | Bus Software Reset Register 4 |
| PS_CTRL_REG | 0x0300 | PS Control Register |
| PS_CNT_REG | 0x0304 | PS Counter Register |

4.3.5. Register Description

4.3.5.1. PLL_CPU Control Register (Default Value: 0x00001000)

| Offset: 0x0000 | | | Register Name: PLL_CPU_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | PLL_ENABLE. 0: Disable 1: Enable The PLL Output= (24MHz*N*K)/(M*P). The PLL output is for the CPUX Clock. Note: The PLL output clock must be in the range of 200MHz~2.6GHz. Its default is 408MHz. |
| 30:29 | / | / | / |
| 28 | R | 0x0 | LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) |
| 27:25 | / | / | / |
| 24 | R/W | 0x0 | CPUX_SDM_EN. 0: Disable 1: Enable |
| 23:18 | / | / | / |
| 17:16 | R/W | 0x0 | PLL_OUT_EXT_DIVP PLL Output external divider P 00: /1 01: /2 10: /4 11: / |

| | | | |
|-------|-----|------|--|
| | | | Note:The P factor only use in the condition that PLL output less than 288 MHz. |
| 15:13 | / | / | / |
| 12:8 | R/W | 0x10 | PLL_FACTOR_N PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 Factor=31, N=32 |
| 7:6 | / | / | / |
| 5:4 | R/W | 0x0 | PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4. |
| 3:2 | / | / | / |
| 1:0 | R/W | 0x0 | PLL_FACTOR_M. PLL Factor M. (M=Factor + 1) The range is from 1 to 4. |

4.3.5.2. PLL_Audio Control Register (Default Value: 0x00035514)

| Offset: 0x0008 | | | Register Name: PLL_AUDIO_CTRL_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | PLL_ENABLE. 0: Disable 1: Enable. The PLL is for Audio. $PLL_AUDIO = (24MHz * N) / (M * P)$ $PLL_AUDIO(8X) = (24MHz * N * 2) / M$ $PLL_AUDIO(4X) = PLL_AUDIO(8X) / 2$ $PLL_AUDIO(2X) = PLL_AUDIO(4X) / 2$ The PLL output clock must be in the range of 20MHz~200MHz. Its default is 24.571MHz. |
| 30:29 | / | / | / |
| 28 | R | 0x0 | LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) |
| 27:25 | / | / | / |
| 24 | R/W | 0x0 | PLL_SDM_EN. 0: Disable 1: Enable In this case, the PLL_FACTOR_N only low 4 bits are valid (N: The range is from 1 to 16). |
| 23:20 | / | / | / |
| 19:16 | R/W | 0x3 | PLL_POSTDIV_P. Post-div factor (P= Factor+1) The range is from 1 to 16. |
| 15 | / | / | / |
| 14:8 | R/W | 0x55 | PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 |

| | | | |
|-----|-----|------|--|
| | | | Factor=127, N=128 |
| 7:5 | / | / | / |
| 4:0 | R/W | 0x14 | PLL_PREDIV_M. PLL Pre-div Factor(M = Factor+1). The range is from 1 to 32. |

4.3.5.3. PLL_VIDEO Control Register (Default Value: 0x03006207)

| Offset: 0x0010 | | | Register Name: PLL_VIDEO_CTRL_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | PLL_ENABLE. 0: Disable 1: Enable In the integer mode,the PLL Output = (24MHz*N)/M. In the fractional mode, the PLL Output is select by bit 25. Note: In the Clock Control Module, PLL(1X) Output=PLL while PLL(2X) Output=PLL * 2. The PLL output clock must be in the range of 30MHz~600MHz. Its default is 297MHz. |
| 30 | R/W | 0x0 | PLL_MODE. 0: Manual Mode 1: Auto Mode (Controlled by DE) |
| 29 | / | / | / |
| 28 | R | 0x0 | LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) |
| 27:26 | / | / | / |
| 25 | R/W | 0x1 | FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); No meaning when PLL_MODE_SEL =1. 0: PLL Output=270MHz 1: PLL Output =297MHz |
| 24 | R/W | 0x1 | PLL_MODE_SEL. 0: Fractional Mode 1: Integer Mode Note: When in Fractional mode, the Per Divider M should be set to 0. |
| 23:21 | / | / | / |
| 20 | R/W | 0x0 | PLL_SDM_EN. 0: Disable 1: Enable |
| 19:15 | / | / | / |
| 14:8 | R/W | 0x62 | PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 Factor=127, N=128 |
| 7:4 | / | / | / |
| 3:0 | R/W | 0x7 | PLL_PREDIV_M. PLL Pre-div Factor(M = Factor+1). |

| | | | |
|--|--|--|----------------------------|
| | | | The range is from 1 to 16. |
|--|--|--|----------------------------|

4.3.5.4. PLL_VE Control Register (Default Value: 0x03006207)

| Offset: 0x0018 | | | Register Name: PLL_VE_CTRL_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | PLL_ENABLE. 0: Disable 1: Enable In the integer mode, The PLL Output = (24MHz*N)/M. In the fractional mode, the PLL Output is select by bit 25. Note: The PLL output clock must be in the range of 30MHz~600MHz. Its default is 297MHz. |
| 30:29 | / | / | / |
| 28 | R | 0x0 | LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) |
| 27:26 | / | / | / |
| 25 | R/W | 0x1 | FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); No meaning when PLL_MODE_SEL =1. 0: PLL Output=270MHz 1: PLL Output =297MHz |
| 24 | R/W | 0x1 | PLL_MODE_SEL. 0: Fractional Mode 1: Integer Mode Note: When in Fractional mode, the Per Divider M should be set to 0. |
| 23:21 | / | / | / |
| 20 | R/W | 0x0 | PLL_SDM_EN. 0: Disable 1: Enable |
| 19:15 | / | / | / |
| 14:8 | R/W | 0x62 | PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 Factor=31, N=32 ... Factor=127, N=128 |
| 7:4 | / | / | / |
| 3:0 | R/W | 0x7 | PLL_PREDIV_M. PLL Pre Divider (M = Factor+1). The range is from 1 to 16. |

4.3.5.5. PLL_DDR0 Control Register (Default Value: 0x00001000)

| Offset: 0x0020 | | | Register Name: PLL_DDR0_CTRL_REG |
|----------------|-----|-------------|----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | PLL_ENABLE. |

| | | | |
|-------|-----|------|--|
| | | | 0: Disable 1: Enable Set bit20 to validate the PLL after this bit is set to 1. The PLL Output = $(24\text{MHz} * N * K) / M$. Note: the PLL output clock must be in the range of 200MHz~2.6GHz. Its default is 408MHz. |
| 30:29 | / | / | / |
| 28 | R | 0x0 | LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) |
| 27:25 | / | / | / |
| 24 | R/W | 0x0 | PLL_SDM_EN. 0: Disable 1: Enable |
| 23:21 | / | / | / |
| 20 | R/W | 0x0 | PLL_DDR_CFG_UPDATE. PLL_DDR Configuration Update. When PLL_DDR has been changed, this bit should be set to 1 to validate the PLL, otherwise the change would be invalid. And this bit would be cleared automatically after the PLL change is valid. 0: No effect 1: Validating the PLL_DDR |
| 19:13 | / | / | / |
| 12:8 | R/W | 0x10 | PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 Factor=31, N=32 |
| 7:6 | / | / | / |
| 5:4 | R/W | 0x0 | PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4. |
| 3:2 | / | / | / |
| 1:0 | R/W | 0x0 | PLL_FACTOR_M. PLL Factor M.(M = Factor + 1) The range is from 1 to 4. |

4.3.5.6. PLL_PERIPH0 Control Register (Default Value: 0x00041811)

| Offset: 0x0028 | | | Register Name: PLL_PERIPH0_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | PLL_ENABLE. 0: Disable 1: Enable The PLL Output = $24\text{MHz} * N * K / 2$. Note: The PLL Output should be fixed to 600MHz, it is not recommended to vary this value arbitrarily. In the Clock Control Module, PLL(2X) output= PLL * 2 = $24\text{MHz} * N * K$. The PLL output clock must be in the range of 200MHz~1.8GHz. Its default is 600MHz. |

| | | | |
|-------|-----|------|--|
| 30:29 | / | / | / |
| 28 | R | 0x0 | LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) |
| 27:26 | / | / | / |
| 25 | R/W | 0x0 | PLL_BYPASS_EN. PLL Output Bypass Enable. 0: Disable 1: Enable If the bypass is enabled, the PLL output is 24MHz. |
| 24 | R/W | 0x0 | PLL_CLK_OUT_EN. PLL clock output enable. 0: Disable 1: Enable |
| 23:19 | / | / | / |
| 18 | R/W | 0x1 | PLL_24M_OUT_EN. PLL 24MHz Output Enable. 0: Disable 1: Enable When 25MHz crystal used, this PLL can output 24MHz. |
| 17:16 | R/W | 0x0 | PLL_24M_POST_DIV. PLL 24M Output Clock Post Divider (When 25MHz crystal used). 1/2/3/4. |
| 15:13 | / | / | / |
| 12:8 | R/W | 0x18 | PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 Factor=31, N=32 |
| 7:6 | / | / | / |
| 5:4 | R/W | 0x1 | PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4. |
| 3:2 | / | / | / |
| 1:0 | R/W | 0x1 | PLL_FACTOR_M. PLL Factor M (M = Factor + 1) is only valid in plltest debug. The PLL_PERIPH back door clock output =24MHz*N*K/M. The range is from 1 to 4. |

4.3.5.7. PLL_ISP Control Register (Default Value: 0x03006207)

| Offset: 0x002C | | | Register Name: PLL_ISP_CTRL_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | PLL_ENABLE. 0: Disable 1: Enable In the integer mode,the PLL Output = (24MHz*N)/M. In the fractional mode, the PLL Output is select by bit 25. Note: In the Clock Control Module, PLL(1X) Output=PLL while PLL(2X) Output=PLL * 2. |

| | | | |
|-------|-----|------|--|
| | | | The PLL output clock must be in the range of 30MHz~600MHz. Its default is 297MHz. |
| 30 | R/W | 0x0 | PLL_MODE. 0: Manual Mode 1: Auto Mode (Controlled by DE) |
| 29 | / | / | / |
| 28 | R | 0x0 | LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) |
| 27:26 | / | / | / |
| 25 | R/W | 0x1 | FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); No meaning when PLL_MODE_SEL =1. 0: PLL Output=270MHz 1: PLL Output =297MHz |
| 24 | R/W | 0x1 | PLL_MODE_SEL. 0: Fractional Mode 1: Integer Mode Note: When in Fractional mode, the Per Divider M should be set to 0. |
| 23:21 | / | / | / |
| 20 | R/W | 0x0 | PLL_SDM_EN. 0: Disable 1: Enable |
| 19:15 | / | / | / |
| 14:8 | R/W | 0x62 | PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 Factor=127,N=128 |
| 7:4 | / | / | / |
| 3:0 | R/W | 0x7 | PLL_PREDIV_M. PLL Pre-div Factor(M = Factor+1). The range is from 1 to 16. |

4.3.5.8. PLL_PERIPH1 Control Register (Default Value: 0x00041811)

| Offset: 0x0044 | | | Register Name: PLL_PERIPH1_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | PLL_ENABLE. 0: Disable 1: Enable The PLL Output = 24MHz*N*K/2. Note: The PLL Output should be fixed to 600MHz, it is not recommended to vary this value arbitrarily. In the Clock Control Module, PLL(2X) output= PLL*2 = 24MHz*N*K. The PLL output clock must be in the range of 200MHz~1.8GHz. Its default is 600MHz. |
| 30:29 | / | / | / |
| 28 | R | 0x0 | LOCK. 0: Unlocked |

| | | | |
|-------|-----|------|--|
| | | | 1: Locked (It indicates that the PLL has been stable.) |
| 27:26 | / | / | / |
| 25 | R/W | 0x0 | PLL_BYPASS_EN. PLL Output Bypass Enable. 0: Disable 1: Enable If the bypass is enabled, the PLL output is 24MHz. |
| 24 | R/W | 0x0 | PLL_CLK_OUT_EN. PLL clock output enable(Just for the SATA Phy) 0: Disable 1: Enable |
| 23:21 | / | / | / |
| 20 | R/W | 0x0 | PLL_SDM_EN. 0: Disable 1: Enable |
| 19 | / | / | / |
| 18 | R/W | 0x1 | PLL_24M_OUT_EN. PLL 24MHz Output Enable. 0: Disable 1: Enable When 25MHz crystal used, this PLL can output 24MHz. |
| 17:16 | R/W | 0x0 | PLL_24M_POST_DIV. PLL 24M Output Clock Post Divider (When 25MHz crystal used). 1/2/3/4. |
| 15:13 | / | / | / |
| 12:8 | R/W | 0x18 | PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 Factor=31, N=32 |
| 7:6 | / | / | / |
| 5:4 | R/W | 0x1 | PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4. |
| 3:2 | / | / | / |
| 1:0 | R/W | 0x1 | PLL_FACTOR_M. PLL Factor M (M = Factor + 1) is only valid in plltest debug. The PLL_PERIPH back door clock output =24MHz*N*K/M. The range is from 1 to 4. |

4.3.5.9. PLL_DDR1 Control Register (Default Value: 0x00001800)

| Offset: 0x004C | | | Register Name: PLL_DDR1_CTRL_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | PLL_ENABLE. 0: Disable 1: Enable. The PLL Output = 24MHz*N/M. Its default is 600 MHz. |
| 30 | R/W | 0x0 | SDRPLL_UPD. |

| | | | |
|-------|-----|------|--|
| | | | SDRPLL Configuration Update. Note: When PLL_DDR1 has changed, this bit should be set to 1 to validate the PLL, otherwise the change is invalid. It will be auto cleared after the PLL is valid. 0: No effect 1: To validate the PLL_DDR1. |
| 29 | / | / | / |
| 28 | R | 0x0 | LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.) |
| 27:25 | / | / | / |
| 24 | R/W | 0x0 | PLL_SDM_EN. 0: Disable 1: Enable. |
| 23:16 | / | / | / |
| 15:8 | R/W | 0x18 | PLL_FACTOR_N. PLL Factor N. (N = Factor + 1) The range is from 0 to 127. Note: Bit 15 can not be accessed. |
| 7:2 | / | / | / |
| 1:0 | R/W | 0x0 | PLL_FACTOR_M. PLL Factor M.(M = Factor + 1) The range is from 1 to 4. |

4.3.5.10. CPU/AXI Configuration Register (Default Value: 0x00010000)

| Offset: 0x0050 | | | Register Name: CPU_AXI_CFG_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:18 | / | / | / |
| 17:16 | R/W | 0x1 | CPU_CLK_SRC_SEL. CPU Clock Source Select. CPU Clock = Clock Source 00: LOSC 01: OSC24M 1X: PLL_CPU If the clock source is changed, at most to wait for 8 present running clock cycles. |
| 15:10 | / | / | / |
| 9:8 | R/W | 0x0 | CPU_APB_CLK_DIV. 00: /1 01: /2 1x: /4 Note: System APB clock source is CPU clock source. |
| 7:2 | / | / | / |
| 1:0 | R/W | 0x0 | AXI_CLK_DIV_RATIO. AXI Clock Divide Ratio. AXI Clock source is CPU clock source. 00: /1 01: /2 10: /3 11: /4 |

4.3.5.11. AHB1/APB1 Configuration Register (Default Value: 0x00001010)

| Offset: 0x0054 | | | Register Name: AHB1_APB1_CFG_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| 13:12 | R/W | 0x1 | AHB1_CLK_SRC_SEL. 00: LOSC 01: OSC24M 10: AXI 11: PLL_PERIPH0/ AHB1_PRE_DIV |
| 11:10 | / | / | / |
| 9:8 | R/W | 0x0 | APB1_CLK_RATIO. APB1 Clock Divide Ratio. APB1 clock source is AHB1 clock. 00: /2 01: /2 10: /4 11: /8 |
| 7:6 | R/W | 0x0 | AHB1_PRE_DIV AHB1 Clock Pre Divide Ratio 00: /1 01: /2 10: /3 11: /4 |
| 5:4 | R/W | 0x1 | AHB1_CLK_DIV_RATIO. AHB1 Clock Divide Ratio. 00: /1 01: /2 10: /4 11: /8 |
| 3:0 | / | / | / |

4.3.5.12. APB2 Configuration Register (Default Value: 0x01000000)

| Offset: 0x0058 | | | Register Name: APB2_CFG_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:26 | / | / | / |
| 25:24 | R/W | 0x1 | APB2_CLK_SRC_SEL. APB2 Clock Source Select 00: LOSC 01: OSC24M 1X: PLL_PERIPH0 This clock is used for some special module apbclk(UART、TWI). Because these modules need special clock rate even if the apb1clk changed. |
| 23:18 | / | / | / |
| 17:16 | R/W | 0x0 | CLK_RAT_N Clock Pre Divide Ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8. |
| 15:5 | / | / | / |
| 4:0 | R/W | 0x0 | CLK_RAT_M. Clock Divide Ratio (m) The Pre Divide clock is divided by (m+1). The divider M is from 1 to 32. |

4.3.5.13. AHB2 Configuration Register (Default Value: 0x00000000)

| Offset: 0x005C | | | Register Name: AHB2_CFG_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:2 | / | / | / |
| 1:0 | R/W | 0x0 | AHB2_CLK_CFG. 00: AHB1 Clock 01: PLL_PERIPH0 / 2 1X: / EMAC ,USB OTG_EHCI/OHCI0 and USBOTG_Device0 default clock source is AHB2 Clock. |

4.3.5.14. Bus Clock Gating Register0 (Default Value: 0x00000000)

| Offset: 0x0060 | | | Register Name: BUS_CLK_GATING_REG0 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:30 | / | / | / |
| 29 | R/W | 0x0 | USBOHCI_GATING. Gating Clock for USB OHCI 0: Mask 1: Pass |
| 28:27 | / | / | / |
| 26 | R/W | 0x0 | USBEHCI_GATING. Gating Clock For USB EHCI 0: Mask 1: Pass |
| 25 | / | / | / |
| 24 | R/W | 0x0 | USB OTG_Device_GATING. Gating Clock For USB OTG_Device 0: Mask 1: Pass |
| 23:21 | / | / | / |
| 20 | R/W | 0x0 | SPI_GATING. Gating Clock For SPI 0: Mask 1: Pass |
| 19 | R/W | 0x0 | HSTMR_GATING. Gating Clock For High Speed Timer 0: Mask 1: Pass |
| 18 | / | / | / |
| 17 | R/W | 0x0 | EMAC_GATING. Gating Clock For EMAC 0: Mask 1: Pass |
| 16:15 | / | / | / |
| 14 | R/W | 0x0 | DRAM_GATING. Gating Clock For DRAM 0: Mask 1: Pass |
| 13:11 | / | / | / |
| 10 | R/W | 0x0 | MMC2_GATING. |

| | | | |
|-----|-----|-----|---|
| | | | Gating Clock For MMC2 0: Mask 1: Pass |
| 9 | R/W | 0x0 | MMC1_GATING. Gating Clock For MMC1 0: Mask 1: Pass |
| 8 | R/W | 0x0 | MMC0_GATING. Gating Clock For MMC0 0: Mask 1: Pass |
| 7 | / | / | / |
| 6 | R/W | 0x0 | DMA_GATING. Gating Clock For DMA 0: Mask 1: Pass |
| 5 | R/W | 0x0 | CE_GATING. Gating Clock For CE. 0: Mask 1: Pass |
| 4:0 | / | / | / |

4.3.5.15. Bus Clock Gating Register1 (Default Value: 0x00000000)

| Offset: 0x0064 | | | Register Name: BUS_CLK_GATING_REG1 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:13 | / | / | / |
| 12 | R/W | 0x0 | DE_GATING. 0: Mask 1: Pass. |
| 11:9 | / | / | / |
| 8 | R/W | 0x0 | CSI_GATING. Gating Clock For CSI 0: Mask 1: Pass |
| 7:5 | / | / | / |
| 4 | R/W | 0x0 | TCON_GATING. Gating Clock For TCON 0: Mask 1: Pass |
| 3:1 | / | / | / |
| 0 | R/W | 0x0 | VE_GATING. Gating Clock For VE 0: Mask 1: Pass |

4.3.5.16. Bus Clock Gating Register2 (Default Value: 0x00000000)

| Offset: 0x0068 | | | Register Name: BUS_CLK_GATING_REG2 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:13 | / | / | / |

| | | | |
|------|-----|-----|---|
| 12 | R/W | 0x0 | I2S/PCM_GATING. Gating Clock For I2S/PCM 0: Mask 1: Pass |
| 11:6 | / | / | / |
| 5 | R/W | 0x0 | PIO_GATING. Gating Clock For PIO 0: Mask 1: Pass |
| 4:1 | / | / | / |
| 0 | R/W | 0x0 | AC_DIG_GATING. Gating Clock For AC Digital 0: Mask 1: Pass |

4.3.5.17. Bus Clock Gating Register3 (Default Value: 0x00000000)

| Offset: 0x006C | | | Register Name: BUS_CLK_GATING_REG3 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:19 | / | / | / |
| 18 | R/W | 0x0 | UART2_GATING. Gating Clock For UART2 0: Mask 1: Pass |
| 17 | R/W | 0x0 | UART1_GATING. Gating Clock For UART1 0: Mask 1: Pass |
| 16 | R/W | 0x0 | UART0_GATING. Gating Clock For UART0 0: Mask 1: Pass |
| 15:2 | / | / | / |
| 1 | R/W | 0x0 | TW11_GATING. Gating Clock For TW11 0: Mask 1: Pass |
| 0 | R/W | 0x0 | TW10_GATING. Gating Clock For TW10 0: Mask 1: Pass |

4.3.5.18. Bus Clock Gating Register4 (Default Value: 0x00000000)

| Offset: 0x0070 | | | Register Name: BUS_CLK_GATING_REG4 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R/W | 0x0 | DBGSYS_GATING. Gating Clock For DBGSYS 0: Mask 1: Pass |

| | | | |
|-----|-----|-----|---|
| 6:1 | / | / | / |
| 0 | R/W | 0x0 | EPHY_GATING. Gating Clock For EPHY 0: Mask 1: Pass |

4.3.5.19. SDMMC0 Clock Register (Default Value: 0x00000000)

| Offset: 0x0088 | | | Register Name: SDMMC0_CLK_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK = Clock Source/Divider N/Divider M. |
| 30:26 | / | / | / |
| 25:24 | R/W | 0x0 | CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0 10: PLL_PERIPH1 11: / |
| 23 | / | / | / |
| 22:20 | R/W | 0x0 | SAMPLE_CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7. |
| 19:18 | / | / | / |
| 17:16 | R/W | 0x0 | CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8. |
| 15:11 | / | / | / |
| 10:8 | R/W | 0x0 | OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7. |
| 7:4 | / | / | / |
| 3:0 | R/W | 0x0 | CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16. |

4.3.5.20. SDMMC1 Clock Register (Default Value: 0x00000000)

| Offset: 0x008C | | | Register Name: SDMMC1_CLK_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF |

| | | | |
|-------|-----|-----|--|
| | | | 1: Clock is ON. |
| 30:26 | / | / | / |
| 25:24 | R/W | 0x0 | CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0 10: PLL_PERIPH1 11: / |
| 23 | / | / | / |
| 22:20 | R/W | 0x0 | SAMPLE_CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7. |
| 19:18 | / | / | / |
| 17:16 | R/W | 0x0 | CLK_DIV_RATIO_N. Clock Pre-Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8. |
| 15:11 | / | / | / |
| 10:8 | R/W | 0x0 | OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7. |
| 7:4 | / | / | / |
| 3:0 | R/W | 0x0 | CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16. |

4.3.5.21. SDMMC2 Clock Register (Default Value: 0x00000000)

| Offset: 0x0090 | | | Register Name: SDMMC2_CLK_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. If SDMMC2 is in old mode, SCLK = Clock Source/Divider N/Divider M. If SDMMC2 is in new mode, SCLK= Clock Source/Divider N/Divider M/2. |
| 30 | R/W | 0x0 | MMC2_MODE_SELECT. 0: Old Mode 1: New Mode. |
| 29:26 | / | / | / |
| 25:24 | R/W | 0x0 | CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0 10: PLL_PERIPH1 11: / |
| 23 | / | / | / |
| 22:20 | R/W | 0x0 | CLK_PHASE_CTR. |

| | | | |
|-------|-----|-----|--|
| | | | Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7. |
| 19:18 | / | / | / |
| 17:16 | R/W | 0x0 | CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8. |
| 15:11 | / | / | / |
| 10:8 | R/W | 0x0 | OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7. |
| 7:4 | / | / | / |
| 3:0 | R/W | 0x0 | CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16. |

4.3.5.22. CE Clock Register (Default Value: 0x00000000)

| Offset: 0x009C | | | Register Name: CE_CLK_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK = Clock Source/Divider N/Divider M. |
| 30:26 | / | / | / |
| 25:24 | R/W | 0x0 | CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0 10: / 11: / |
| 23:18 | / | / | / |
| 17:16 | R/W | 0x0 | CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8. |
| 15:4 | / | / | / |
| 3:0 | R/W | 0x0 | CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16. |

4.3.5.23. SPI Clock Register (Default Value: 0x00000000)

| Offset: 0x00A0 | | | Register Name: SPI_CLK_REG |
|----------------|--|--|----------------------------|
|----------------|--|--|----------------------------|

| Bit | R/W | Default/Hex | Description |
|-------|-----|-------------|--|
| 31 | R/W | 0x0 | SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK = Clock Source/Divider N/Divider M. |
| 30:26 | / | / | / |
| 25:24 | R/W | 0x0 | CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0 10: PLL_PERIPH1 11: / |
| 23:18 | / | / | / |
| 17:16 | R/W | 0x0 | CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8. |
| 15:4 | / | / | / |
| 3:0 | R/W | 0x0 | CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16. |

4.3.5.24. I2S/PCM Clock Register (Default Value: 0x00000000)

| Offset: 0x00B0 | | | Register Name: I2S/PCM_CLK_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK= Clock Source PLL_AUDIO/Divider M. |
| 30:18 | / | / | / |
| 17:16 | R/W | 0x0 | CLK_SRC_SEL. 00: PLL_AUDIO (8X) 01: PLL_AUDIO(8X)/2 10: PLL_AUDIO(8X)/4 11: PLL_AUDIO |
| 15:0 | / | / | / |

4.3.5.25. USBPHY Configuration Register (Default Value: 0x00000000)

| Offset: 0x00CC | | | Register Name: USBPHY_CFG_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:17 | / | / | / |
| 16 | R/W | 0x0 | SCLK_GATING_OHCI0. Gating Special Clock For OHCI0 0: Clock is OFF 1: Clock is ON |

| | | | |
|------|-----|-----|--|
| 15:9 | / | / | / |
| 8 | R/W | 0x0 | SCLK_GATING_USBPHY0. Gating Special Clock For USB PHY0 0: Clock is OFF 1: Clock is ON |
| 7:1 | / | / | / |
| 0 | R/W | 0x0 | USBPHY0_RST. USB PHY0 Reset Control 0: Assert 1: De-assert |

4.3.5.26. DRAM Configuration Register (Default Value: 0x00000001)

| Offset: 0x00F4 | | | Register Name: DRAM_CFG_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | DRAM_CTR_RST. DRAM Controller Reset For AHB Clock Domain. 0: Assert 1: De-assert. |
| 30:22 | / | / | / |
| 21:20 | R/W | 0x0 | CLK_SRC_SEL. 00: PLL_DDR0 01: PLL_DDR1 10: PLL_PERIPH0 (2X) 11: / |
| 19:17 | / | / | / |
| 16 | R/W | 0x0 | SDRCLK_UPD. SDRCLK Configuration Update. 0:Invalid 1:Valid. Note: Set this bit will validate Configuration 0 . It will be auto cleared after the Configuration 0 is valid. The DRAMCLK Source is from PLL_DDR. |
| 15:4 | / | / | / |
| 3:0 | R/W | 0x1 | DRAM_DIV_M. DRAMCLK Divider of Configuration. The clock is divided by (m+1). The divider M should be from 2 to 16. |

4.3.5.27. PLL_DDR1 Configuration Register (Default Value: 0x00000030)

| Offset: 0x00F8 | | | Register Name: PLL_DDR_CFG_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:13 | / | / | / |
| 12 | R/W | 0x0 | PLL_DDR1_MODE. 0: Normal Mode 1: Continuously Frequency Scale |
| 11:7 | / | / | / |
| 6:4 | R/W | 0x3 | PLL_DDR1_PHASE_COMPENSATE. The value of bit[6:4] is based on 24M clock, then the default PLL_DDR phase compensate is (3/24000000) s. |
| 3:0 | R/W | 0x0 | PLL_DDR1_STEP. |

| | | | |
|--|--|--|--|
| | | | 0000: 0.004MHz/us ($576/2^{17}$) 0001: 0.008MHz/us ($576/2^{16}$) 0010: 0.016MHz/us ($576/2^{15}$) 0011: 0.032MHz/us ($576/2^{14}$) 0100: 0.064MHz/us ($576/2^{13}$) 0101: 0.128MHz/us ($576/2^{12}$) 0110: 0.256MHz/us ($576/2^{11}$) 0111: 0.512MHz/us ($576/2^{10}$) 1000: 1.024MHz/us ($576/2^9$) 1001: 2.048MHz/us ($576/2^8$) Others: 0.004MHz/us ($576/2^{17}$) |
|--|--|--|--|

4.3.5.28. MBUS Reset Register (Default Value: 0x80000000)

| Offset: 0x00FC | | | Register Name: MBUS_RST_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x1 | MBUS_RESET. 0: Reset Mbus Domain 1: Assert Mbus Domain. |
| 30:0 | / | / | / |

4.3.5.29. DRAM Clock Gating Register (Default Value: 0x00000000)

| Offset: 0x0100 | | | Register Name: DRAM_CLK_GATING_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:19 | / | / | / |
| 18 | R/W | 0x0 | USB_OHCI_DCLK_GATING. Gating DRAM Clock For USB OHCI 0: Mask 1: Pass |
| 17 | R/W | 0x0 | USB_EHCI_DCLK_GATING. Gating DRAM Clock For USB EHCI 0: Mask 1: Pass |
| 16:2 | / | / | / |
| 1 | R/W | 0x0 | CSI_DCLK_GATING. Gating DRAM Clock For CSI 0: Mask 1: Pass |
| 0 | R/W | 0x0 | VE_DCLK_GATING. Gating DRAM Clock For VE 0: Mask 1: Pass |

4.3.5.30. DE Clock Gating Register (Default Value: 0x00000000)

| Offset: 0x0104 | | | Register Name: DE_CLK_REG |
|----------------|-----|-------------|----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SCLK_GATING. |

| | | | |
|-------|-----|-----|---|
| | | | Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M. |
| 30:27 | / | / | / |
| 26:24 | R/W | 0x0 | CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO 010: PLL_PERIPH0 Others: / |
| 23:4 | / | / | / |
| 3:0 | R/W | 0x0 | CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16. |

4.3.5.31. TCON Clock Register (Default Value: 0x00000000)

| Offset: 0x0118 | | | Register Name: TCON_CLK_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M. |
| 30:27 | / | / | / |
| 26:24 | R/W | 0x0 | CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO 001: PLL_PERIPH0 Others: / |
| 23:4 | / | / | / |
| 3:0 | R/W | 0x0 | CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16. |

4.3.5.32. CSIO Clock Register (Default Value: 0x00000000)

| Offset: 0x0130 | | | Register Name: CSIO_CLK_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | CSI_MISC_SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = OSC24M. |
| 30:16 | / | / | / |
| 15 | R/W | 0x0 | CSIO_MCLK_GATING. Gating Master Clock 0: Clock is OFF 1: Clock is ON SCLK = CSIO Master Clock Source/ CSIO_MCLK_DIV_M. |
| 14:11 | / | / | / |

| | | | |
|------|-----|-----|---|
| 10:8 | R/W | 0x0 | CSIO_MCLK_SRC_SEL. CSIO Master Clock Source Select 000: OSC24M 001: PLL_VIDEO 010: PLL_PERIPH1 011: PLL_PERIPH0 Others: / |
| 7:5 | / | / | / |
| 4:0 | R/W | 0x0 | CSIO_MCLK_DIV_M. CSIO Master Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32. |

4.3.5.33. CSI1 Clock Register (Default Value: 0x00000000)

| Offset: 0x0134 | | | Register Name: CSI1_CLK_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | CSI_TOP_SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Special Clock Source/CSI_SCLK_DIV_M. |
| 30:27 | / | / | / |
| 26:24 | R/W | 0x0 | SCLK_SRC_SEL. Special Clock Source Select 000: PLL_VIDEO 001: PLL_ISP Others: / |
| 23:20 | / | / | / |
| 19:16 | R/W | 0x0 | CSI_SCLK_DIV_M. CSI Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16. |
| 15 | R/W | 0x0 | CSI1_MCLK_GATING. Gating Master Clock 0: Clock is OFF 1: Clock is ON SCLK =CSI1 Master Clock Source/ CSI1_MCLK_DIV_M. |
| 14:11 | / | / | / |
| 10:8 | R/W | 0x0 | CSI1_MCLK_SRC_SEL. CSI1 Master Clock Source Select 000: OSC24M 001: PLL_VIDEO 010: PLL_PERIPH1 011: PLL_PERIPH0 Others: / |
| 7:5 | / | / | / |
| 4:0 | R/W | 0x0 | CSI1_MCLK_DIV_M. CSI1 Master Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32. |

4.3.5.34. VE Clock Register (Default Value: 0x00000000)

| Offset: 0x013C | | | Register Name: VE_CLK_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | VE_SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK = PLL_VE /Divider N. |
| 30:19 | / | / | /. |
| 18:16 | R/W | 0x0 | CLK_DIV_RATIO_N. Clock Pre Divide Ratio (N) The select clock source is pre-divided by n+1. The divider N is from 1 to 8. |
| 15:0 | / | / | / |

4.3.5.35. AC Digital Clock Register (Default Value: 0x00000000)

| Offset: 0x0140 | | | Register Name: AC_DIG_CLK_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SCLK_1X_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = PLL_AUDIO Output. |
| 30:0 | / | / | / |

4.3.5.36. AVS Clock Register (Default Value: 0x00000000)

| Offset: 0x0144 | | | Register Name: AVS_CLK_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK= OSC24M. |
| 30:0 | / | / | / |

4.3.5.37. MBUS Clock Register (Default Value: 0x00000000)

| Offset: 0x015C | | | Register Name: MBUS_CLK_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| | | | MBUS_SCLK_GATING. Gating Clock for MBUS 0: Clock is OFF 1: Clock is ON. |
| 31 | R/W | 0x0 | MBUS_CLOCK = Clock Source/Divider M |
| 30:26 | / | / | / |
| 25:24 | R/W | 0x0 | MBUS_SCLK_SRC |

| | | | |
|------|-----|-----|--|
| | | | Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X) 10: PLL_DDR0 11: / |
| 23:3 | / | / | / |
| 2:0 | R/W | 0x0 | MBUS_SCLK_RATIO_M Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 8. The divide ratio must be changed smoothly. Note: If the clock has been changed ,it must wait for at least 16 cycles. |

4.3.5.38. MIPI_CSI Register (Default Value: 0x00000000)

| Offset: 0x016C | | | Register Name: MIPI_CSI_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | MIPICSI2_DPHY_CLK_GATING. Gating Clock For CSI_DPHY 0: Clock is OFF 1: Clock is ON SCLK= Clock Source/Divider M |
| 30:26 | / | / | / |
| 25:24 | R/W | 0x0 | CLK_SRC_SEL. Clock Source Select 00: PLL_VIDEO 01: PLL_PERIPH0 10: PLL_ISP 11: / |
| 23:3 | / | / | / |
| 3:0 | R/W | 0x0 | CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16. |

4.3.5.39. PLL Stable Time Register0 (Default Value: 0x000000FF)

| Offset: 0x0200 | | | Register Name: PLL_STABLE_TIME_REG0 |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:16 | / | / | / |
| 15:0 | R/W | 0x00FF | PLL_LOCK_TIME PLL Lock Time (Unit: us). Note: When any PLL (except PLL_CPU) is enabled or changed, the corresponding PLL lock bit will be set after the PLL STABLE Time. |

4.3.5.40. PLL Stable Time Register1 (Default Value: 0x000000FF)

| Offset: 0x0204 | | | Register Name: PLL_STABLE_TIME_REG1 |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:16 | / | / | / |
| 15:0 | R/W | 0x00FF | PLL_CPU_LOCK_TIME |

| | | | |
|--|--|--|--|
| | | | PLL_CPU Lock Time (Unit: us). Note: When PLL_CPU is enabled or changed, the PLL_CPU lock bit will be set after the PLL_CPU STABLE Time. |
|--|--|--|--|

4.3.5.41. PLL_CPUX Bias Register (Default Value: 0x08100200)

| Offset: 0x0220 | | | Register Name: PLL_CPUX_BIAS_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | VCO_RST. VCO reset in. |
| 30:29 | / | / | / |
| 28 | R/W | 0x0 | EXG_MODE. Exchange Mode. Note: CPU PLL source will select PLL_PERIPH0 instead of PLL_CPU |
| 27:24 | R/W | 0x8 | PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[3:0]. |
| 23:21 | / | / | / |
| 20:16 | R/W | 0x10 | PLL_BIAS_CUR_CTRL. PLL Bias Current Control[4:0]. |
| 15:11 | / | / | / |
| 10:8 | R/W | 0x2 | PLL_LOCK_CTRL. PLL Lock Time Control[2:0]. |
| 7:4 | / | / | / |
| 3:0 | R/W | 0x0 | PLL_DAMP_FACT_CTRL. PLL Damping Factor Control[3:0]. |

4.3.5.42. PLL_AUDIO Bias Register (Default Value: 0x10100000)

| Offset: 0x0224 | | | Register Name: PLL_AUDIO_BIAS_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:24 | R/W | 0x10 | PLL_VCO_BIAS. PLL VCO Bias Current[4:0]. |
| 23:21 | / | / | / |
| 20:16 | R/W | 0x10 | PLL_BIAS_CUR. PLL Bias Current[4:0]. |
| 15:0 | / | / | / |

4.3.5.43. PLL_VIDEO Bias Register (Default Value: 0x10100000)

| Offset: 0x0228 | | | Register Name: PLL_VIDEO_BIAS_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:24 | R/W | 0x10 | PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0]. |
| 23:21 | / | / | / |
| 20:16 | R/W | 0x10 | PLL_BIAS_CTRL. PLL Bias Control[4:0]. |

| | | | |
|------|-----|-----|---|
| 15:3 | / | / | / |
| 2:0 | R/W | 0x0 | PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0]. |

4.3.5.44. PLL_VE Bias Register (Default Value: 0x10100000)

| Offset: 0x022C | | | Register Name: PLL_VE_BIAS_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:24 | R/W | 0x10 | PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0]. |
| 23:21 | / | / | / |
| 20:16 | R/W | 0x10 | PLL_BIAS_CTRL. PLL Bias Control[4:0]. |
| 15:3 | / | / | / |
| 2:0 | R/W | 0x0 | PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0]. |

4.3.5.45. PLL_DDR0 Bias Register (Default Value: 0x81104000)

| Offset: 0x0230 | | | Register Name: PLL_DDR0_BIAS_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:28 | R/W | 0x8 | PLL_VCO_BIAS. PLL VCO Bias[3:0]. |
| 27:26 | / | / | /. |
| 25 | R/W | 0x0 | PLL_VCO_GAIN_CTRL_EN. PLL VCO Gain Control Enable. 0: Disable 1: Enable. |
| 24 | R/W | 0x1 | PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide. |
| 23:21 | / | / | / |
| 20:16 | R/W | 0x10 | PLL_BIAS_CUR_CTRL. PLL Bias Current Control. |
| 15 | / | / | / |
| 14:12 | R/W | 0x4 | PLL_VCO_GAIN_CTRL. PLL VCO Gain Control Bit[2:0]. |
| 11:4 | / | / | / |
| 3:0 | R/W | 0x0 | PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[3:0]. |

4.3.5.46. PLL_PERIPH0 Bias Register (Default Value: 0x10100010)

| Offset: 0x0234 | | | Register Name: PLL_PERIPH0_BIAS_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |

| | | | |
|-------|-----|------|--|
| 28:24 | R/W | 0x10 | PLL_VCO_BIAS. PLL VCO Bias[4:0]. |
| 23:21 | / | / | / |
| 20:16 | R/W | 0x10 | PLL_BIAS_CUR_CTRL. PLL Bias Current Control. |
| 15:5 | / | / | / |
| 4 | R/W | 0x1 | PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide |
| 3:2 | / | / | / |
| 1:0 | R/W | 0x0 | PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[1:0]. |

4.3.5.47. PLL_ISP Bias Register (Default Value: 0x10100000)

| Offset: 0x0238 | | | Register Name: PLL_ISP_BIAS_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:24 | R/W | 0x10 | PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0]. |
| 23:21 | / | / | / |
| 20:16 | R/W | 0x10 | PLL_BIAS_CTRL. PLL Bias Control[4:0]. |
| 15:3 | / | / | / |
| 2:0 | R/W | 0x0 | PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0]. |

4.3.5.48. PLL_PERIPH1 Bias Register (Default Value: 0x10100010)

| Offset: 0x0244 | | | Register Name: PLL_PERIPH1_BIAS_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:24 | R/W | 0x10 | PLL_VCO_BIAS. PLL VCO Bias[4:0]. |
| 23:21 | / | / | / |
| 20:16 | R/W | 0x10 | PLL_BIAS_CUR_CTRL. PLL Bias Current Control. |
| 15:5 | / | / | / |
| 4 | R/W | 0x1 | PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide |
| 3:2 | / | / | / |
| 1:0 | R/W | 0x0 | PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[1:0]. |

4.3.5.49. PLL_DDR1 Bias Register (Default Value: 0x10010000)

| Offset: 0x024C | | | Register Name: PLL_DDR1_BIAS_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:24 | R/W | 0x10 | PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0]. |
| 23:21 | / | / | / |
| 20:16 | R/W | 0x01 | PLL_BIAS_CUR_CTRL. PLL Bias Current Control[4:0]. |
| 15:0 | / | / | / |

4.3.5.50. PLL_CPU Tuning Register (Default Value: 0x0A101000)

| Offset: 0x0250 | | | Register Name: PLL_CPU_TUN_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| 27 | R/W | 0x1 | PLL_BAND_WID_CTRL. PLL Band Width Control. 0: Narrow 1: Wide |
| 26 | R/W | 0x0 | VCO_GAIN_CTRL_EN. VCO Gain Control Enable. 0: Disable 1: Enable |
| 25:23 | R/W | 0x4 | VCO_GAIN_CTRL. VCO Gain Control Bits[2:0]. |
| 22:16 | R/W | 0x10 | PLL_INIT_FREQ_CTRL. PLL Initial Frequency Control[6:0]. |
| 15 | R/W | 0x0 | C_OD. C-Reg-Od For Verify. |
| 14:8 | R/W | 0x10 | C_B_IN. C-B-In[6:0] For Verify. |
| 7 | R/W | 0x0 | C_OD1. C-Reg-Od1 For Verify. |
| 6:0 | R | 0x0 | C_B_OUT. C-B-Out[6:0] For Verify. |

4.3.5.51. PLL_DDR0 Tuning Register (Default Value: 0x14880000)

| Offset: 0x0260 | | | Register Name: PLL_DDR0_TUN_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28 | R/W | 0x1 | VREG1_OUT_EN. Vreg1 Out Enable. 0: Disable 1: Enable |
| 27 | / | / | / |
| 26:24 | R/W | 0x4 | PLL_LTIME_CTRL. PLL Lock Time Control[2:0]. |

| | | | |
|-------|-----|------|--|
| 23 | R/W | 0x1 | VCO_RST. VCO Reset In. |
| 22:16 | R/W | 0x08 | PLL_INIT_FREQ_CTRL. PLL Initial Frequency Control[6:0]. |
| 15 | R/W | 0x0 | OD1. Reg-Od1 For Verify. |
| 14:8 | R/W | 0x0 | B_IN. B-In[6:0] For Verify. |
| 7 | R/W | 0x0 | OD. Reg-Od For Verify. |
| 6:0 | R | 0x0 | B_OUT. B-Out[6:0] For Verify. |

4.3.5.52. PLL_CPU Pattern Control Register (Default Value: 0x00000000)

| Offset: 0x0280 | | | Register Name: PLL_CPU_PAT_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SIG_DELT_PAT_EN. Sigma-delta Pattern Enable. |
| 30:29 | R/W | 0x0 | SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular |
| 28:20 | R/W | 0x0 | WAVE_STEP. Wave Step. |
| 19 | / | / | / |
| 18:17 | R/W | 0x0 | FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz |
| 16:0 | R/W | 0x0 | WAVE_BOT. Wave Bottom. |

4.3.5.53. PLL_AUDIO Pattern Control Register(Default Value: 0x00000000)

| Offset: 0x0284 | | | Register Name: PLL_AUDIO_PAT_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SIG_DELT_PAT_EN. Sigma-delta Pattern Enable. |
| 30:29 | R/W | 0x0 | SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular |
| 28:20 | R/W | 0x0 | WAVE_STEP. Wave Step. |
| 19 | / | / | / |

| | | | |
|-------|-----|-----|---|
| 18:17 | R/W | 0x0 | FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz |
| 16:0 | R/W | 0x0 | WAVE_BOT. Wave Bottom. |

4.3.5.54. PLL_VIDEO Pattern Control Register (Default Value: 0x00000000)

| Offset: 0x0288 | | | Register Name: PLL_VIDEO_PAT_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SIG_DELT_PAT_EN. Sigma-delta Pattern Enable. |
| 30:29 | R/W | 0x0 | SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular |
| 28:20 | R/W | 0x0 | WAVE_STEP. Wave Step. |
| 19 | / | / | / |
| 18:17 | R/W | 0x0 | FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz |
| 16:0 | R/W | 0x0 | WAVE_BOT. Wave Bottom. |

4.3.5.55. PLL_VE Pattern Control Register (Default Value: 0x00000000)

| Offset: 0x028C | | | Register Name: PLL_VE_PAT_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SIG_DELT_PAT_EN. Sigma-delta Pattern Enable. |
| 30:29 | R/W | 0x0 | SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular |
| 28:20 | R/W | 0x0 | WAVE_STEP. Wave Step. |
| 19 | / | / | / |
| 18:17 | R/W | 0x0 | FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz |

| | | | |
|------|-----|-----|---------------------------|
| | | | 11: 33KHz |
| 16:0 | R/W | 0x0 | WAVE_BOT. Wave Bottom. |

4.3.5.56. PLL_DDR0 Pattern Control Register (Default Value: 0x00000000)

| Offset: 0x0290 | | | Register Name: PLL_DDR0_PAT_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SIG_DELT_PAT_EN. Sigma-delta Pattern Enable. |
| 30:29 | R/W | 0x0 | SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular |
| 28:20 | R/W | 0x0 | WAVE_STEP. Wave step. |
| 19 | / | / | / |
| 18:17 | R/W | 0x0 | FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz |
| 16:0 | R/W | 0x0 | WAVE_BOT. Wave Bottom. |

4.3.5.57. PLL_ISP Pattern Control Register (Default Value: 0x00000000)

| Offset: 0x0298 | | | Register Name: PLL_ISP_PAT_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SIG_DELT_PAT_EN. Sigma-delta Pattern Enable. |
| 30:29 | R/W | 0x0 | SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular |
| 28:20 | R/W | 0x0 | WAVE_STEP. Wave step. |
| 19 | / | / | / |
| 18:17 | R/W | 0x0 | FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz |
| 16:0 | R/W | 0x0 | WAVE_BOT. Wave Bottom. |

4.3.5.58. PLL_PERIPH1 Pattern Control Register (Default Value: 0x00000000)

| Offset: 0x02A4 | | | Register Name: PLL_PERIPH1_PAT_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable. |
| 30:29 | R/W | 0x0 | SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular |
| 28:20 | R/W | 0x0 | WAVE_STEP. Wave Step. |
| 19 | / | / | / |
| 18:17 | R/W | 0x0 | FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz |
| 16:0 | R/W | 0x0 | WAVE_BOT. Wave Bottom. |

4.3.5.59. PLL_DDR1 Pattern Control Register (Default Value: 0x00000000)

| Offset: 0x02AC | | | Register Name: PLL_DDR1_PAT_CTRL_REG0 |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable. |
| 30:29 | R/W | 0x0 | SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular |
| 28:20 | R/W | 0x0 | WAVE_STEP. Wave Step. |
| 19 | / | / | / |
| 18:17 | R/W | 0x0 | FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz |
| 16:0 | R/W | 0x0 | WAVE_BOT. Wave Bottom. |

4.3.5.60. PLL_DDR1 Pattern Control Register1 (Default Value: 0x00000000)

| Offset: 0x02B0 | | | Register Name: PLL_DDR1_PAT_CTRL_REG1 |
|----------------|-----|-------------|---------------------------------------|
| Bit | R/W | Default/Hex | Description |

| | | | |
|-------|-----|-----|------------|
| 30:25 | / | / | / |
| 24 | R/W | 0x0 | DITHER_EN. |
| 23:21 | / | / | / |
| 20 | R/W | 0x0 | FRAC_EN. |
| 19:17 | / | / | / |
| 16:0 | R/W | 0x0 | FRAC_IN. |

4.3.5.61. Bus Software Reset Register 0 (Default Value: 0x00000000)

| Offset: 0x02C0 | | | Register Name: BUS_SOFT_RST_REG0 |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:30 | / | / | / |
| 29 | R/W | 0x0 | USBOHCI_RST. USB OHCI Reset Control 0: Assert 1: De-assert |
| 27:28 | / | / | / |
| 26 | R/W | 0x0 | USBEHCI_RST. USB EHCI Reset Control 0: Assert 1: De-assert |
| 25 | / | / | / |
| 24 | R/W | 0x0 | USB_OTG_Device_RST. USB OTG_Device Reset Control 0: Assert 1: De-assert |
| 23:21 | / | / | / |
| 20 | R/W | 0x0 | SPI_RST. SPI Reset. 0: Assert 1: De-assert |
| 19 | R/W | 0x0 | HSTMR_RST. HSTMR Reset. 0: Assert 1: De-assert |
| 18 | / | / | / |
| 17 | R/W | 0x0 | EMAC_RST. EMAC Reset. 0: Assert 1: De-assert |
| 16:15 | / | / | / |
| 14 | R/W | 0x0 | SDRAM_RST. SDRAM AHB Reset. 0: Assert 1: De-assert |
| 13:11 | / | / | / |
| 10 | R/W | 0x0 | SD2_RST. SD/MMC2 Reset. 0: Assert 1: De-assert |
| 9 | R/W | 0x0 | SD1_RST. SD/MMC1 Reset. |

| | | | |
|-----|-----|-----|---|
| | | | 0: Assert 1: De-assert |
| 8 | R/W | 0x0 | SD0_RST. SD/MMCO Reset. 0: Assert 1: De-assert |
| 7 | / | / | / |
| 6 | R/W | 0x0 | DMA_RST. DMA Reset. 0: Assert 1: De-assert |
| 5 | R/W | 0x0 | CE_RST. CE Reset. 0: Assert 1: De-assert |
| 4:0 | / | / | / |

4.3.5.62. Bus Software Reset Register 1 (Default Value: 0x00000000)

| Offset: 0x02C4 | | | Register Name: BUS_SOFT_RST_REG1 |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | DBGSYS_RST. DBGSYS Reset 0: Assert 1: De-assert |
| 30:13 | / | / | / |
| 12 | R/W | 0x0 | DE_RST. DE Reset. 0: Assert 1: De-assert |
| 11:9 | / | / | / |
| 8 | R/W | 0x0 | CSI_RST. CSI Reset. 0: Assert 1: De-assert |
| 7:5 | / | / | / |
| 4 | R/W | 0x0 | TCON_RST. TCON Reset. 0: Assert 1: De-assert |
| 3:1 | / | / | / |
| 0 | R/W | 0x0 | VE_RST. VE Reset. 0: Assert 1: De-assert |

4.3.5.63. Bus Software Reset Register 2 (Default Value: 0x00000000)

| Offset: 0x02C8 | | | Register Name: BUS_SOFT_RST_REG2 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:3 | / | / | / |

| | | | |
|---|-----|-----|---|
| 2 | R/W | 0x0 | EPHY_RST. EPHY Reset. 0: Assert 1: De-assert |
| 1 | / | / | / |
| 0 | R/W | 0x0 | LVDS_RST. LVDS Reset. 0: Assert 1: De-assert |

4.3.5.64. Bus Software Reset Register 3 (Default Value: 0x00000000)

| Offset: 0x02D0 | | | Register Name: BUS_SOFT_RST_REG3 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:13 | / | / | / |
| 12 | R/W | 0x0 | I2S/PCM_RST. I2S/PCM Reset. 0: Assert 1: De-assert. |
| 11:1 | / | / | / |
| 0 | R/W | 0x0 | AC_DIG_RST. AC Digital Reset. 0: Assert 1: De-assert |

4.3.5.65. Bus Software Reset Register 4 (Default Value: 0x00000000)

| Offset: 0x02D8 | | | Register Name: BUS_SOFT_RST_REG4 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:19 | / | / | / |
| 18 | R/W | 0x0 | UART2_RST. UART2 Reset. 0: Assert 1: De-assert |
| 17 | R/W | 0x0 | UART1_RST. UART1 Reset. 0: Assert 1: De-assert |
| 16 | R/W | 0x0 | UART0_RST. UART0 Reset. 0: Assert 1: De-assert |
| 15:2 | / | / | / |
| 1 | R/W | 0x0 | TWI1_RST. TWI1 Reset. 0: Assert 1: De-assert |
| 0 | R/W | 0x0 | TWI0_RST. TWI0 Reset. 0: Assert 1: De-assert |

4.3.5.66. PS Control Register (Default Value: 0x00000000)

| Offset: 0x0300 | | | Register Name: PS_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R/W | 0x0 | DET_FIN. Detect Finish. 0: Unfinished 1: Finished Set 1 to this bit will clear it. |
| 6 | R/W | 0x0 | DLY_SEL. Delay Select 0: 1 Cycle 1: 2 Cycles |
| 5:4 | R/W | 0x0 | OSC_SEL OSC Select. 00: IDLE 01: SVT 10: LVT 11: ULVT |
| 3:1 | R/W | 0x0 | TIME_DET. Time detect. 000: 0.5/4 us 001: 0.5/2 us 010: 0.5/1 us 011: 0.5*2us 111:0.5*2^5us |
| 0 | R/W | 0x0 | MOD_EN. Module enable. 0: Disable 1: Enable |

4.3.5.67. PS Counter Register (Default Value: 0x00000000)

| Offset: 0x0304 | | | Register Name: PS_CNT_REG |
|----------------|-----|-------------|----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:16 | / | / | / |
| 15:0 | R/W | 0x0 | PS_CNT. PS Counter. |

4.3.6. Programming Guidelines
4.3.6.1. PLL

- 1) In practical application, other PLLs doesn't support dynamic frequency scaling except for PLL_CPU and PLL_DDR1;
- 2) After the PLL_DDR0 frequency changes, the 20-bit of PLL_DDR0 Control Register should be written 1 to make it valid;
- 3) After the PLL_DDR1 frequency changes, the 30-bit of PLL_DDR1 Control Register should be written 1 to make it valid.

4.3.6.2. BUS

- 1) When setting the BUS clock , you should set the division factor first, and after the division factor becomes valid, switch the clock source. The clock source will be switched after at least three clock cycles;
- 2) The BUS clock should not be dynamically changed in most applications.

4.3.6.3. Clock Switch

Make sure that the clock source output is valid before the clock source switch, and then set a proper divide ratio; after the division factor becomes valid, switch the clock source.

4.3.6.4. Gating and reset

Make sure that the reset signal has been released before the release of module clock gating;

4.4. System Control

4.4.1. Overview

| Area | Size(Bytes) |
|--------------|-------------|
| SRAM A1 | 16K |
| SRAM C | 44K |
| CPU I-Cache | 32K |
| CPU D-Cache | 32K |
| CPU L2 Cache | 128K |
| Total | 252K |

4.4.2. System Control Register List

| Module Name | Base Address |
|----------------|--------------|
| System Control | 0x01C00000 |

| Register Name | Offset | Description |
|---------------|--------|--------------------------|
| VER_REG | 0x24 | Version Register |
| EMAC_CLK_REG | 0x30 | EMAC -EPHYClock Register |

4.4.3. System Control Register Description

4.4.3.1. Version Register

| Offset:0x24 | | | Register Name: VER_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:9 | / | / | / |
| 8 | R | x | UBOOT_SEL_PAD_STA U_boot Select Pin Status 0: U_Boot 1: Normal Boot |
| 7:0 | R | 0x0 | VER_BITS This read-only bit field always reads back the mask revision level of the chip. |

4.4.3.2. EMAC-EPHY Clock Register (Default Value: 0x00058000)

| Offset:0x30 | | | Register Name: EMAC_EPHY_CLK_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | R/W | 0x0 | BPS_EFFUSE |
| 27 | R/W | 0x0 | XMII_SEL 0: Internal SMI and MII 1: External SMI and MII |
| 26:25 | R/W | 0x0 | EPHY_MODE Operation Mode Selection 00 : Normal Mode |

| | | | |
|-------|-----|-----|---|
| | | | 01 : Sim Mode 10 : AFE Test Mode 11 : / |
| 24:20 | R/W | 0x0 | PHY_ADDR PHY Address |
| 19 | R/W | 0x0 | BIST_CLK_EN 0 : BIST clk disable 1 : BIST clk enable |
| 18 | R/W | 0x1 | CLK_SEL 0 : 25MHz 1 : 24MHz |
| 17 | R/W | 0x0 | LED_POL 0 : High active 1 : Low active |
| 16 | R/W | 0x1 | SHUTDOWN 0 : Power up 1 : Shutdown |
| 15 | R/W | 0x1 | PHY_SELECT. 0 : External PHY 1 : Internal PHY |
| 14 | / | / | / |
| 13 | R/W | 0x0 | RMII_EN 0 : Disable RMII Module 1 : Enable RMII Module When this bit assert, MII or RGMII interface is disabled(This means bit13 is prior to bit2) |
| 12:10 | R/W | 0x0 | ETXDC Configure EMAC Transmit Clock Delay Chain. |
| 9:5 | R/W | 0x0 | ERXDC Configure EMAC Receive Clock Delay Chain. |
| 4 | R/W | 0x0 | ERXIE Enable EMAC Receive Clock Invertor. 0: Disable 1: Enable |
| 3 | R/W | 0x0 | ETXIE Enable EMAC Transmit Clock Invertor. 0: Disable 1: Enable |
| 2 | R/W | 0x0 | EPIT EMAC PHY Interface Type 0: MII 1: RGMII |
| 1:0 | R/W | 0x0 | ETCS EMAC Transmit Clock Source 00: Transmit clock source for MII 01: External transmit clock source for GMII and RGMII 10: Internal transmit clock source for GMII and RGMII 11: Reserved |

4.5. Timer

4.5.1. Overview

Timer 0/1/2 can take their inputs from Internal OSC or OSC24M. They provide the operating system’s scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 24-bit programmable overflow counter and work in auto-reload mode or no-reload mode. When the current value in *Current Value Register* is counting down to zero, the timer will generate interrupt if set interrupt enable bit.

The watchdog is used to resume the controller operation when it had been disturbed by malfunctions such as noise and system errors. It features a down counter that allows a watchdog period of up to 16 seconds (512000 cycles). It can generate a general reset or interrupt request.

AVS counter is used to synchronize video and audio in the player.

4.5.2. Block Diagram

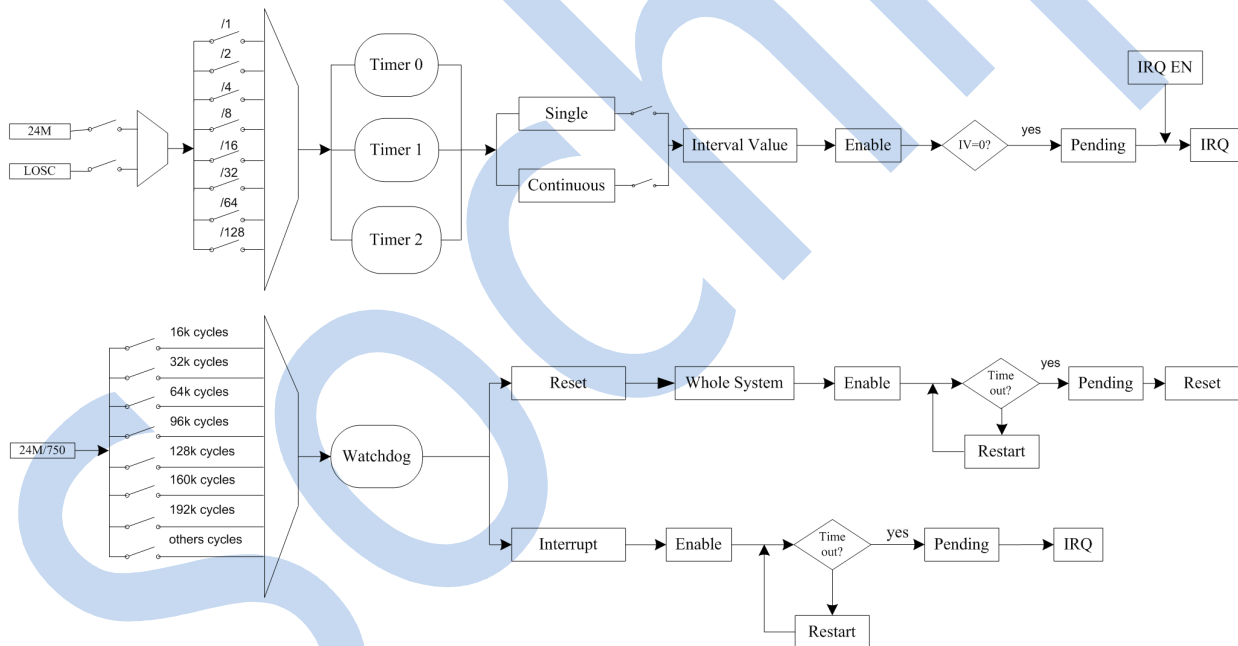


Figure 4-4. Timer Block Diagram

4.5.3. Timer Register List

| Module Name | Base Address |
|-------------|--------------|
| TIMER | 0x01C20C00 |

| Register Name | Offset | Description |
|-----------------|--------|---------------------------|
| TMR_IRQ_EN_REG | 0x0 | Timer IRQ Enable Register |
| TMR_IRQ_STA_REG | 0x4 | Timer Status Register |
| TMR0_CTRL_REG | 0x10 | Timer 0 Control Register |

| | | |
|---------------------|------|-----------------------------------|
| TMR0_INTV_VALUE_REG | 0x14 | Timer 0 Interval Value Register |
| TMR0_CUR_VALUE_REG | 0x18 | Timer 0 Current Value Register |
| TMR1_CTRL_REG | 0x20 | Timer 1 Control Register |
| TMR1_INTV_VALUE_REG | 0x24 | Timer 1 Interval Value Register |
| TMR1_CUR_VALUE_REG | 0x28 | Timer 1 Current Value Register |
| TMR2_CTRL_REG | 0x30 | Timer 2 Control Register |
| TMR2_INTV_VALUE_REG | 0x34 | Timer 2 Interval Value Register |
| TMR2_CUR_VALUE_REG | 0x38 | Timer 2 Current Value Register |
| AVS_CNT_CTL_REG | 0x80 | AVS Control Register |
| AVS_CNT0_REG | 0x84 | AVS Counter 0 Register |
| AVS_CNT1_REG | 0x88 | AVS Counter 1 Register |
| AVS_CNT_DIV_REG | 0x8C | AVS Divisor Register |
| WDOG_IRQ_EN_REG | 0xA0 | Watchdog IRQ Enable Register |
| WDOG_IRQ_STA_REG | 0xA4 | Watchdog Status Register |
| WDOG_CTRL_REG | 0xB0 | Watchdog Control Register |
| WDOG_CFG_REG | 0xB4 | Watchdog Configuration Register |
| WDOG_MODE_REG | 0xB8 | Watchdog Mode Register |
| CNT64_TEST_REG | 0xD0 | 64-bit Counter Test Mode Register |
| CNT64_CTRL_REG | 0xD4 | 64-bit Counter Control Register |
| CNT64_LOW_REG | 0xD8 | 64-bit Counter Low Register |
| CNT64_HIGH_REG | 0xDC | 64-bit Counter High Register |

4.5.4. Timer Register Description

4.5.4.1. Timer IRQ Enable Register (Default Value: 0x00000000)

| Offset:0x0 | | | Register Name: TMR_IRQ_EN_REG |
|------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:3 | / | / | / |
| 2 | R/W | 0x0 | TMR2_IRQ_EN. Timer 2 Interrupt Enable. 0: No effect; 1: Timer 2 Interval Value reached interrupt enable. |
| 1 | R/W | 0x0 | TMR1_IRQ_EN. Timer 1 Interrupt Enable. 0: No effect; 1: Timer 1 Interval Value reached interrupt enable. |
| 0 | R/W | 0x0 | TMRO_IRQ_EN. Timer 0 Interrupt Enable. 0: No effect; 1: Timer 0 Interval Value reached interrupt enable. |

4.5.4.2. Timer IRQ Status Register (Default Value: 0x00000000)

| Offset:0x04 | | | Register Name: TMR_IRQ_STA_REG |
|-------------|-----|-------------|---------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:3 | / | / | / |

| | | | |
|---|-----|-----|---|
| 2 | R/W | 0x0 | TMR2_IRQ_PEND. Timer 2 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, timer 2 interval value is reached. |
| 1 | R/W | 0x0 | TMR1_IRQ_PEND. Timer 1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, timer 1 interval value is reached. |
| 0 | R/W | 0x0 | TMRO_IRQ_PEND. Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, timer 0 interval value is reached. |

4.5.4.3. Timer 0 Control Register (Default Value: 0x00000004)

| Offset:0x10 | | | Register Name: TMRO_CTRL_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R/W | 0x0 | TMRO_MODE. Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically. |
| 6:4 | R/W | 0x0 | TMRO_CLK_PRES. Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 |
| 3:2 | R/W | 0x1 | TMRO_CLK_SRC. Timer 0 Clock Source. 00: Internal OSC / 512 01: OSC24M. 10: / 11: / Internal OSC / N is about 32KHz. |
| 1 | R/W | 0x0 | TMRO_RELOAD. Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value. After the bit is set, it can not be written again before it's cleared automatically. |
| 0 | R/W | 0x0 | TMRO_EN. Timer 0 Enable. 0: Stop/Pause 1: Start. When the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the |

| | | | |
|--|--|--|--|
| | | | current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state; the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time. |
|--|--|--|--|

4.5.4.4. Timer 0 Interval Value Register

| Offset:0x14 | | | Register Name: TMRO_INTV_VALUE_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | TMRO_INTV_VALUE. Timer 0 Interval Value. Note: The value setting should consider the system clock and the timer clock source. |

4.5.4.5. Timer 0 Current Value Register

| Offset:0x18 | | | Register Name: TMRO_CUR_VALUE_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | TMRO_CUR_VALUE. Timer 0 Current Value. Note: It is a 32-bit down-counter (from interval value to 0). |

4.5.4.6. Timer 1 Control Register (Default Value: 0x00000004)

| Offset:0x20 | | | Register Name: TMR1_CTRL_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R/W | 0x0 | TMR1_MODE. Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically. |
| 6:4 | R/W | 0x0 | TMR1_CLK_PRES. Select the pre-scale of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 |
| 3:2 | R/W | 0x1 | TMR1_CLK_SRC. 00: Internal OSC / 512 01: OSC24M. 10: / |

| | | | |
|---|-----|-----|--|
| | | | 11: /. Internal OSC / N is about 32KHz. |
| 1 | R/W | 0x0 | TMR1_RELOAD. Timer 1 Reload. 0: No effect 1: Reload timer 1 Interval value. After the bit is set, it can not be written again before it's cleared automatically. |
| 0 | R/W | 0x0 | TMR1_EN. Timer 1 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time. |

4.5.4.7. Timer 1 Interval Value Register

| Offset:0x24 | | | Register Name: TMR1_INTV_VALUE_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | TMR1_INTV_VALUE. Timer 1 Interval Value. Note: The value setting should consider the system clock and the timer clock source. |

4.5.4.8. Timer 1 Current Value Register

| Offset:0x28 | | | Register Name: TMR1_CUR_VALUE_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | TMR1_CUR_VALUE. Timer 1 Current Value. It is a 32-bit down-counter (from interval value to 0). |

4.5.4.9. Timer 2 Control Register

| Offset:0x30 | | | Register Name: TMR2_CTRL_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R/W | 0x0 | TMR2_MODE. Timer 2 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable |

| | | | |
|-----|-----|-----|--|
| | | | automatically. |
| 6:4 | R/W | 0x0 | TMR2_CLK_PRES. Select the pre-scale of timer 2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 |
| 3:2 | R/W | 0x1 | TMR2_CLK_SRC. 00: Internal OSC / 512 01: OSC24M. 10: / 11: /. |
| 1 | R/W | 0x0 | TMR2_RELOAD. Timer 2 Reload. 0: No effect, 1: Reload timer 2 Interval value. After the bit is set, it can not be written again before it's cleared automatically. |
| 0 | R/W | 0x0 | TMR2_EN. Timer 2 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time. |

4.5.4.10. Timer 2 Interval Value Register

| Offset:0x34 | | | Register Name: TMR2_INTV_VALUE_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | TMR2_INTV_VALUE. Timer 2 Interval Value. Note: The value setting should consider the system clock and the timer clock source. |

4.5.4.11. Timer 2 Current Value Register

| Offset:0x38 | | | Register Name: TMR2_CUR_VALUE_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | TMR2_CUR_VALUE. Timer 2 Current Value. Note: Timer 2 current value is a 32-bit down-counter (from interval value to 0). |

4.5.4.12. AVS Counter Control Register (Default Value: 0x00000000)

| Offset:0x80 | | | Register Name: AVS_CNT_CTL_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:10 | / | / | / |
| 9 | R/W | 0x0 | AVS_CNT1_PS. Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1. |
| 8 | R/W | 0x0 | AVS_CNT0_PS. Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0. |
| 7:2 | / | / | / |
| 1 | R/W | 0x0 | AVS_CNT1_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable. |
| 0 | R/W | 0x0 | AVS_CNT0_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable. |

4.5.4.13. AVS Counter 0 Register (Default Value: 0x00000000)

| Offset:0x84 | | | Register Name: AVS_CNT0_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | AVS_CNT0. Counter 0 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to '1'. When it is paused, the counter won't increase. |

4.5.4.14. AVS Counter 1 Register (Default Value: 0x00000000)

| Offset:0x88 | | | Register Name: AVS_CNT1_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | AVS_CNT1. Counter 1 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, |

| | | | |
|--|--|--|-----------------------------|
| | | | the counter won't increase. |
|--|--|--|-----------------------------|

4.5.4.15. AVS Counter Divisor Register (Default Value: 0x05DB05DB)

| Offset:0x8C | | | Register Name: AVS_CNT_DIV_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| 27:16 | R/W | 0x5DB | AVS_CNT1_D. Divisor N for AVS Counter 1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit [27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches ($\geq N$) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. Note: It can be configured by software at any time. |
| 15:12 | / | / | / |
| 11:0 | R/W | 0x5DB | AVS_CNT0_D. Divisor N for AVS Counter 0 AVS CN0 CLK=24MHz/Divisor_NO. Divisor NO = Bit [11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches ($\geq N$) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. Note: It can be configured by software at any time. |

4.5.4.16. Watchdog IRQ Enable Register (Default Value: 0x00000000)

| Offset:0xA0 | | | Register Name: WDOG_IRQ_EN_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | WDOG_IRQ_EN. Watchdog Interrupt Enable. 0: No effect 1: Watchdog0 interrupt enable. |

4.5.4.17. Watchdog Status Register (Default Value: 0x00000000)

| Offset:0xA4 | | | Register Name: WDOG_IRQ_STA_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | WDOG_IRQ_PEND. Watchdog IRQ Pending. Set 1 to the bit will clear it. |

| | | | |
|--|--|--|---|
| | | | 0: No effect, 1: Pending, watchdog0 interval value is reached. |
|--|--|--|---|

4.5.4.18. Watchdog Control Register (Default Value: 0x00000000)

| Offset:0xB0 | | | Register Name: WDOG_CTRL_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:13 | / | / | / |
| 12:1 | R/W | 0x0 | WDOG_KEY_FIELD. Watchdog Key Field. Should be written at value 0xA57. Writing any other value in this field aborts the write operation. |
| 0 | R/W | 0x0 | WDOG_RSTART. Watchdog Restart. 0: No effect, 1: Restart watchdog. |

4.5.4.19. Watchdog Configuration Register (Default Value: 0x00000001)

| Offset:0xB4 | | | Register Name: WDOG_CFG_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:2 | / | / | / |
| 1:0 | R/W | 0x1 | WDOG_CONFIG. Watchdog generates a reset signal 00: / 01: To whole system 10: Only interrupt 11: / |

4.5.4.20. Watchdog Mode Register (Default Value: 0x00000000)

| Offset:0xB8 | | | Register Name: WDOG_MODE_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:4 | R/W | 0x0 | WDOG_INTV_VALUE. Watchdog Interval Value Watchdog clock source is <i>OSC24M / 750</i> . If the clock source is turned off, Watchdog will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) |

| | | | |
|-----|-----|-----|--|
| | | | 1011: 512000 cycles (16s) others: / |
| 3:1 | / | / | / |
| 0 | R/W | 0x0 | WDOG_EN. Watchdog Enable. 0: No effect; 1: Enable watchdog. |

4.5.4.21. 64-bit Counter Control Register (Default Value: 0x00000000)

| Offset:0xD0 | | | Register Name: CNT64_CTRL_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | CNT64_TEST_EN. 64-bit Counter Test Mode Enable. 0: Normal Mode, 1: Test Mode. In the Test Mode, this Counter Low/Hi registers will count simultaneously. |
| 30:3 | / | / | /. |
| 2 | R/W | 0x0 | CNT64_CLK_SRC_SEL. 64-bit Counter Clock Source Select. 0: OSC24M 1: / |
| 1 | R/W | 0x0 | CNT64_RL_EN. 64-bit Counter Read Latch Enable. 0: no effect, 1: to latch the 64-bit Counter to the Low/Hi registers and it will change to zero after the registers are latched. |
| 0 | R/W | 0x0 | CNT64_CLR_EN. 64-bit Counter Clear Enable. 0: no effect, 1: to clear the 64-bit Counter Low/Hi registers and it will change to zero after the registers are cleared. Note: It is not recommended to clear this counter arbitrarily. |

4.5.4.22. 64-bit Counter Low Register (Default Value: 0x00000000)

| Offset:0xD4 | | | Register Name: CNT64_LOW_REG |
|-------------|-----|-------------|-------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | CNT64_LO. 64-bit Counter [31:0]. |

4.5.4.23. 64-bit Counter High Register (Default Value: 0x00000000)

| Offset:0xD8 | | | Register Name: CNT64_HIGH_REG |
|-------------|-----|-------------|--------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | CNT64_HI. 64-bit Counter [63:32]. |

4.6. High-speed Timer

4.6.1. Overview

High Speed Timer Clock Source is fixed to AHBCLK, which is much higher than OSC24M. Compared with other timers, High Speed Timer clock source is synchronized with AHB clock, and when the relevant bit in the Control Register is set 1, timer goes into the test mode, which is used to System Simulation. When the current value in both LO and HI Current Value Register are counting down to zero, the timer will generate interrupt if set interrupt enable bit.

The High Speed Timer includes the following features:

- 56-bit counter
- Clock source is synchronized with AHB clock, which means calculating much more accurate than other timers

4.6.2. Operation Principle

4.6.2.1. HSTimer clock gating and software reset

By default the HSTimer clock gating is mask. When it is necessary to use HSTimer, its clock gating should be open in **BUS Clock Gating Register0** and then de-assert the software reset in **BUS Software Reset Register0** on CCU module. If it is no need to use HSTimer, both the gating bit and software reset bit should be set 0.

4.6.2.2. HSTimer reload bit

Differing from the reload of Timer, when interval value is reloaded into current value register, the reload bit would not turn to 0 automatically until you clear it. If software hopes the current value register to down-count from the new interval value in pause status, the reload bit and the enable bit should be written 1 at the same time.

4.6.3. HSTimer Register List

| Module Name | Base Address | |
|------------------|--------------|--|
| High Speed Timer | 0x01C60000 | |

| Register Name | Offset | Description |
|----------------------|--------|--|
| HS_TMR_IRQ_EN_REG | 0x00 | HS Timer IRQ Enable Register |
| HS_TMR_IRQ_STAS_REG | 0x04 | HS Timer Status Register |
| HS_TMR0_CTRL_REG | 0x10 | HS Timer0 Control Register |
| HS_TMR0_INTV_LO_REG | 0x14 | HS Timer0 Interval Value Low Register |
| HS_TMR0_INTV_HI_REG | 0x18 | HS Timer0 Interval Value High Register |
| HS_TMR0_CURNT_LO_REG | 0x1C | HS Timer0 Current Value Low Register |
| HS_TMR0_CURNT_HI_REG | 0x20 | HS Timer0 Current Value High Register |
| HS_TMR1_CTRL_REG | 0x30 | HS Timer1 Control Register |
| HS_TMR1_INTV_LO_REG | 0x34 | HS Timer1 Interval Value Low Register |
| HS_TMR1_INTV_HI_REG | 0x38 | HS Timer1 Interval Value High Register |
| HS_TMR1_CURNT_LO_REG | 0x3C | HS Timer1 Current Value Low Register |

| | | |
|----------------------|------|---------------------------------------|
| HS_TMR1_CURNT_HI_REG | 0x40 | HS Timer1 Current Value High Register |
|----------------------|------|---------------------------------------|

4.6.4. HSTimer Register Description

4.6.4.1. HS Timer IRQ Enable Register (Default Value: 0x00000000)

| Offset:0x0 | | | Register Name: HS_TMR_IRQ_EN_REG |
|------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:2 | / | / | / |
| 1 | R/W | 0x0 | HS_TMR1_INT_EN. High Speed Timer1 Interrupt Enable. 0: No effect; 1: High Speed Timer1 Interval Value reached interrupt enable. |
| 0 | R/W | 0x0 | HS_TMRO_INT_EN. High Speed Timer0 Interrupt Enable. 0: No effect; 1: High Speed Timer0 Interval Value reached interrupt enable. |

4.6.4.2. HS Timer IRQ Status Register (Default Value: 0x00000000)

| Offset:0x4 | | | Register Name: HS_TMR_IRQ_STAS_REG |
|------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:2 | / | / | / |
| 1 | R/W | 0x0 | HS_TMR1_IRQ_PEND. High Speed Timer1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, High speed timer interval value is reached. |
| 0 | R/W | 0x0 | HS_TMRO_IRQ_PEND. High Speed Timer0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, High speed timer interval value is reached. |

4.6.4.3. HS Timer0 Control Register (Default Value: 0x00000000)

| Offset:0x10 | | | Register Name: HS_TMRO_CTRL_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | HS_TMRO_TEST. High speed timer0 test mode. In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: normal mode; 1: test mode. |
| 30:8 | / | / | / |
| 7 | R/W | 0x0 | HS_TMRO_MODE. High Speed Timer0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically. |

| | | | |
|-----|-----|-----|---|
| 6:4 | R/W | 0x0 | HS_TMRO_CLK Select the pre-scale of the high speed timer0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: / |
| 3:2 | / | / | / |
| 1 | R/W | 0x0 | HS_TMRO_RELOAD. High Speed Timer0 Reload. 0: No effect, 1: Reload High Speed Timer0 Interval Value. |
| 0 | R/W | 0x0 | HS_TMRO_EN. High Speed Timer0 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time. |

4.6.4.4. HS Timer0 Interval Value Lo Register

| | | | |
|-------------|-----|-------------|---|
| Offset:0x14 | | | Register Name: HS_TMRO_INTV_LO_REG |
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | x | HS_TMRO_INTV_VALUE_LO. High Speed Timer Interval Value [31:0]. |

4.6.4.5. HS Timer0 Interval Value Hi Register

| | | | |
|-------------|-----|-------------|---|
| Offset:0x18 | | | Register Name: HS_TMRO_INTV_HI_REG |
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:0 | R/W | x | HS_TMRO_INTV_VALUE_HI. High Speed Timer0 Interval Value [55:32]. |

Note:The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or write first. And the Hi register should be written after the Lo register.

4.6.4.6. HS Timer0 Current Value Lo Register

| | | | |
|-------------|-----|-------------|--|
| Offset:0x1C | | | Register Name: HS_TMRO_CURNT_LO_REG |
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | x | HS_TMRO_CUR_VALUE_LO. |

| | | | |
|--|--|--|---|
| | | | High Speed Timer0 Current Value [31:0]. |
|--|--|--|---|

4.6.4.7. HS Timer0 Current Value Hi Register

| Offset:0x20 | | | Register Name: HS_TMR0_CURNT_HI_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:0 | R/W | x | HS_TMR0_CUR_VALUE_HI. High Speed Timer0 Current Value [55:32]. |

Note 1:HS Timer0 current value is a 56-bit down-counter (from interval value to 0).

Note2:The current value register is a 56-bit register. When read or write the current value, the Lo register should be read or write first.

4.6.4.8. HS Timer1 Control Register (Default Value: 0x00000000)

| Offset:0x30 | | | Register Name: HS_TMR1_CTRL_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | HS_TMR1_TEST. High speed timer1 test mode. In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: normal mode; 1: test mode. |
| 30:8 | / | / | / |
| 7 | R/W | 0x0 | HS_TMR1_MODE. High Speed Timer1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically. |
| 6:4 | R/W | 0x0 | HS_TMR1_CLK Select the pre-scale of the high speed timer1 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: / |
| 3:2 | / | / | / |
| 1 | R/W | 0x0 | HS_TMR1_RELOAD. High Speed Timer1 Reload. 0: No effect, 1: Reload High Speed Timer1 Interval Value. |
| 0 | R/W | 0x0 | HS_TMR1_EN. High Speed Timer1 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. |

| | | | |
|--|--|--|--|
| | | | In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time. |
|--|--|--|--|

4.6.4.9. HS Timer1 Interval Value Lo Register

| Offset:0x34 | | | Register Name: HS_TMR1_INTV_LO_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | x | HS_TMR0_INTV_VALUE_LO. High Speed Timer Interval Value [31:0]. |

4.6.4.10. HS Timer1 Interval Value Hi Register

| Offset:0x38 | | | Register Name: HS_TMR1_INTV_HI_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:0 | R/W | x | HS_TMR1_INTV_VALUE_HI. High Speed Timer1 Interval Value [55:32]. |

Note: The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or write first. And the Hi register should be written after the Lo register.

4.6.4.11. HS Timer1 Current Value Lo Register

| Offset:0x3C | | | Register Name: HS_TMR1_CURNT_LO_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | x | HS_TMR1_CUR_VALUE_LO. High Speed Timer1 Current Value [31:0]. |

4.6.4.12. HS Timer1 Current Value Hi Register

| Offset:0x40 | | | Register Name: HS_TMR1_CURNT_HI_REG |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:0 | R/W | x | HS_TMR1_CUR_VALUE_HI. High Speed Timer1 Current Value [55:32]. |

Note1: HS timer1 current value is a 56-bit down-counter (from interval value to 0).

Note2: The current value register is a 56-bit register. When read or write the current value, the Lo register should be read or write first.

4.6.5. Programming Guidelines

Take making a 1us delay using HSTimer for an instance as follow, AHB1CLK will be configured as 100MHz and n_mode, Single mode and 2 pre-scale will be selected in this instance.

```
writel(0x0, HS_TMR_INTV_HI); //Set interval value Hi 0x0
writel(0x32, HS_TMR_INTV_LO); //Set interval value Lo 0x32
writel(0x90, HS_TMR_CTRL); //Select n_mode,2 pre-scale,single mode
writel(readl(HS_TMR_CTRL)|(1<<1), HS_TMR_CTRL); //Set Reload bit
writel(readl(HS_TMR_CTRL)|(1<<0), HS_TMR_CTRL); //Enable HSTimer
While(!(readl(HS_TMR_IRQ_STAT)&1)); //Wait for HSTimer to generate pending
Writel(1,HS_TMR_IRQ_STAT); //Clear HSTimer pending
```

Sochip

4.7. PWM

4.7.1. Overview

The output of the PWM is a toggling signal whose frequency and duty cycle can be modulated by its programmable registers. Each channel has a dedicated internal 16-bit up counter. If the counter reaches the value stored in the channel period register, it resets. At the beginning of a count period cycle, the PWMOUT is set to active state and count from 0x0000. The PWM divider divides the clock (24MHz) by 1~4096 according to the pre-scalar bits in the PWM control register.

In PWM cycle mode, the output will be a square waveform, the frequency is set to the period register. In PWM pulse mode, the output will be a positive pulse or a negative pulse.

4.7.2. Functionalities Description

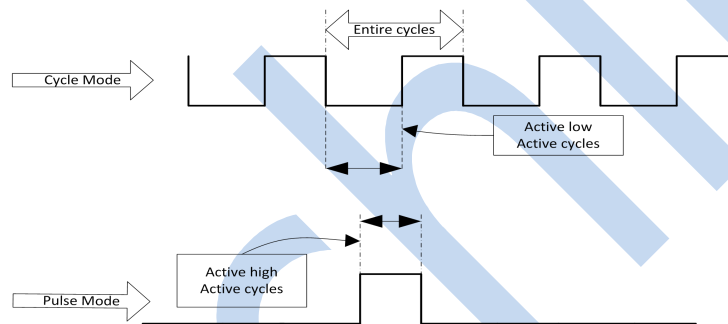


Figure 4-5. PWM Block Diagram

When PWM is enabling, the PWM can output two signals, which are reversed on two pins. And when PWM is disabling, the PWM can control the status of two pins. The PWM divider divides the clock (24MHz) by 1-64 according to the pre-scalar bits in the PWM control register. The PWM output Frequency can be divided by 65536 at most. In PWM cycle mode, the output will be a square waveform; the frequency is set to the period register. In PWM pulse mode, the output will be a positive pulse or a negative pulse.

4.7.3. PWM Register List

| Module Name | Base Address |
|-------------|--------------|
| PWM | 0x01C21400 |

| Register Name | Offset | Description |
|----------------|--------|-------------------------------|
| PWM_CH_CTRL | 0x00 | PWM Control Register |
| PWM_CH0_PERIOD | 0x04 | PWM Channel 0 Period Register |
| PWM_CH1_PERIOD | 0x08 | PWM Channel 1 Period Register |

4.7.4. PWM Register Description

4.7.4.1. PWM Control Register(Default Value: 0x00000000)

| Offset:0x0 | | | Register Name: PWM_CTRL_REG |
|------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:30 | / | / | /. |
| 29 | RO | 0x0 | PWM1_RDY. PWM1 period register ready. 0: PWM1 period register is ready to write, 1: PWM1 period register is busy. |
| 28 | RO | 0x0 | PWM0_RDY. PWM0 period register ready. 0: PWM0 period register is ready to write, 1: PWM0 period register is busy. |
| 27:25 | / | / | / |
| 24 | R/W | 0x0 | PWM1_BYPASS. PWM CH1 bypass enable. If the bit is set to 1, PWM1's output is OSC24MHz. 0: disable 1: enable |
| 23 | R/W | 0x0 | PWM_CH1_PULSE_OUT_START. PWM Channel 1 pulse output start. 0: no effect, 1: output 1 pulse. The pulse width should be according to the period 1 register[15:0],and the pulse state should be according to the active state. After the pulse is finished, the bit will be cleared automatically. |
| 22 | R/W | 0x0 | PWM_CH1_MODE. PWM Channel 1 mode. 0: cycle mode, 1: pulse mode. |
| 21 | R/W | 0x0 | PWM_CH1_CLK_GATING Gating the Special Clock for PWM1(0: mask, 1: pass). |
| 20 | R/W | 0x0 | PWM_CH1_ACT_STATE. PWM Channel 1 Active State. 0: Low Level, 1: High Level. |
| 19 | R/W | 0x0 | PWM_CH1_EN. PWM Channel 1 Enable. 0: Disable, 1: Enable. |
| 18:15 | R/W | 0x0 | PWM_CH1_PRESCAL. PWM Channel 1 Prescaler. These bits should be setting before the PWM Channel 1 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360 0100: /480 0101: / 0110: / 0111: / |

| | | | |
|-------|-----|-----|---|
| | | | 1000: /12k 1001: /24k 1010: /36k 1011: /48k 1100: /72k 1101: / 1110: / 1111: /1 |
| 14:10 | / | / | / |
| 9 | R/W | 0x0 | PWM0_BYPASS. PWM CH0 bypass enable. If the bit is set to 1, PWM0's output is OSC24MHz. 0: disable, 1: enable. |
| 8 | R/W | 0x0 | PWM_CH0_PUL_START. PWM Channel 0 pulse output start. 0: no effect, 1: output 1 pulse. The pulse width should be according to the period 0 register[15:0],and the pulse state should be according to the active state. After the pulse is finished,the bit will be cleared automatically. |
| 7 | R/W | 0x0 | PWM_CHANNEL0_MODE. 0: cycle mode, 1: pulse mode. |
| 6 | R/W | 0x0 | SCLK_CH0_GATING. Gating the Special Clock for PWM0(0: mask, 1: pass). |
| 5 | R/W | 0x0 | PWM_CH0_ACT_STA. PWM Channel 0 Active State. 0: Low Level, 1: High Level. |
| 4 | R/W | 0x0 | PWM_CH0_EN. PWM Channel 0 Enable. 0: Disable, 1: Enable. |
| 3:0 | R/W | 0x0 | PWM_CH0_PRESCAL. PWM Channel 0 Prescalar. These bits should be setting before the PWM Channel 0 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360 0100: /480 0101: / 0110: / 0111: / 1000: /12k 1001: /24k 1010: /36k 1011: /48k 1100: /72k 1101: / 1110: / 1111: /1 |

4.7.4.2. PWM Channel 0 Period Register

| Offset:0x4 | | | Register Name: PWM_CH0_PERIOD |
|------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | R/W | x | PWM_CH0_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK (PWM CLK = 24MHz/pre-scale). |
| 15:0 | R/W | x | PWM_CH0_ENTIRE_ACT_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles N = N cycles |

Note:The active cycles should be no larger than the period cycles.

4.7.4.3. PWM Channel 1 Period Register

| Offset:0x8 | | | Register Name: PWM_CH1_PERIOD |
|------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | R/W | x | PWM_CH1_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK (PWM CLK = 24MHz/pre-scale). |
| 15:0 | R/W | x | PWM_CH1_ENTIRE_ACT_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles N = N cycles |

Note:The active cycles should be no larger than the period cycles.

4.8. DMA

4.8.1. Overview

There are 8 DMA channels in the chip. Each DMA channel can generate interrupts. According to different pending status, the referenced DMA channel generates corresponding interrupt. And, the configuration information of every DMA channel are storing in the DDR or SRAM. When start a DMA transferring, the **DMA Channel Descriptor Address Register** contains the address information in the DDR or SRAM, where has the relevance configuration information of the DMA transferring.

4.8.2. Functionalities Description

4.8.2.1. Block Diagram

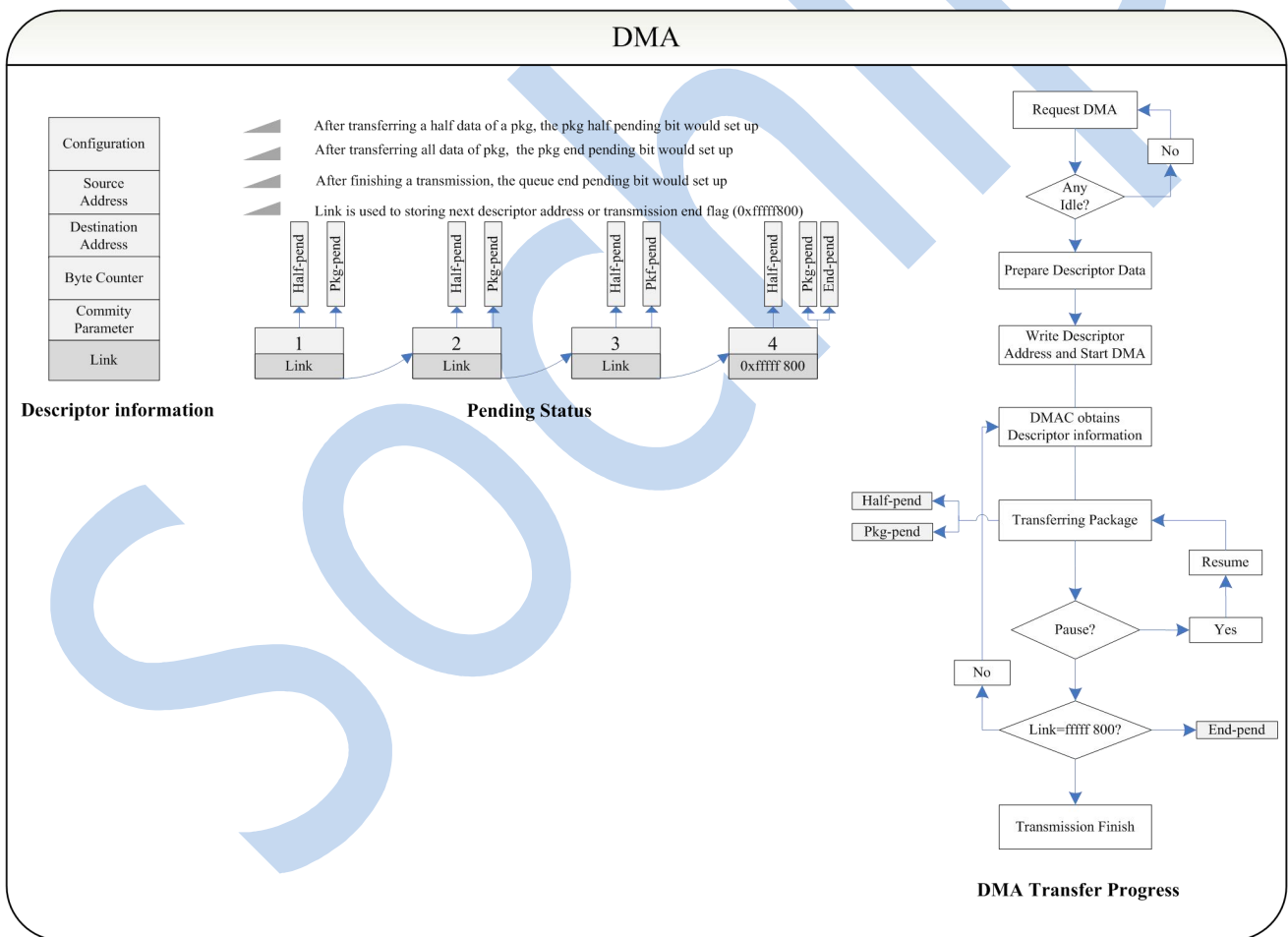


Figure 4-6. DMA Block Diagram

4.8.2.2. DRQ Type and Corresponding Relation

Table 4-1. DMA DRQ Table

| Source DRQ Type | | Destination DRQ Type | |
|-----------------|-------------|----------------------|-------------|
| Port NO. | Module Name | Port NO. | Module Name |
| Port 0 | SRAM | Port 0 | SRAM |

| | | | |
|---------|--------------------|---------|--------------------|
| Port 1 | SDRAM | Port 1 | SDRAM |
| Port 2 | | Port 2 | |
| Port 3 | I2S/PCM_RX | Port 3 | I2S/PCM_TX |
| Port 4 | | Port 4 | |
| Port 5 | | Port 5 | |
| Port 6 | UART0_RX | Port 6 | UART0_TX |
| Port 7 | UART1_RX | Port 7 | UART1_TX |
| Port 8 | UART2_RX | Port 8 | UART2_TX |
| Port 9 | / | Port 9 | / |
| Port 10 | / | Port 10 | / |
| Port 11 | / | Port 11 | / |
| Port 12 | / | Port 12 | / |
| Port 13 | / | Port 13 | / |
| Port 14 | / | Port 14 | / |
| Port 15 | CODEC | Port 15 | CODEC |
| Port 16 | CE_RX | Port 16 | CE_TX |
| Port 17 | USB OTG_Device_EP1 | Port 17 | USB OTG_Device_EP1 |
| Port 18 | USB OTG_Device_EP2 | Port 18 | USB OTG_Device_EP2 |
| Port 19 | USB OTG_Device_EP3 | Port 19 | USB OTG_Device_EP3 |
| Port20 | USB OTG_Device_EP4 | Port 20 | USB OTG_Device_EP4 |
| Port 21 | / | Port 21 | / |
| Port 22 | / | Port 22 | / |
| Port 23 | SPI_RX | Port 23 | SPI_TX |
| Port 24 | | Port 24 | |
| Port 25 | | Port 25 | |
| Port 26 | | Port 26 | |
| Port 27 | | Port 27 | |
| Port 28 | | Port 28 | |
| Port 29 | | Port 29 | |
| Port 30 | | Port 30 | |

4.8.2.3. DMA Descriptor

In this section, the DMA descriptor registers will be introduced in detail.

When starting a DMA transmission, the module data are transferred as packages, which have the link data information. And, by reading the DMA Status Register, the status of a DMA channel could be known. Reading back the descriptor address register, the value is the link data in the transferring package. If only the value is equal to 0xffff800, then it can be regarded as NULL, which means the package is the last package in this DMA transmission. Otherwise, the value means the start address of the next package. And, the Descriptor Address Register can be changed during a package transferring.

When transferring the half of a package, the relevant pending bit will be set up automatically, and if the corresponding interrupt is enabled, DMA generates an interrupt to the system. The similar thing would occur when transferring a package completely. Meanwhile, if DMA have transferred the last package in the data, the relevant pending bit would be set up, and generates an interrupt if the corresponding interrupt is enabled. The flow-process diagram is showed in Block Diagram section.

During a DMA transmission, the configuration could be obtained via the Configuration Register. And, behind the address of the config register in DDR or SRAM, there are some registers including other information of a DMA transmission. The structure chart is showed in Block Diagram section. Also, other information of a transferring data can be obtained by reading the Current Source Address Register, Current Destination Address Register and Byte Counter Left Register. The

configuration must be word-aligning.

The transferring data would be paused when setting up the relevant Pause Register, if coming up emergency. And the pausing data could be presumable when set 0 to the same bit in Pause Register.

4.8.3. DMA Register List

| Module Name | Base Address |
|-------------|--------------|
| DMA | 0x01C02000 |

| Register Name | Offset | Description |
|-------------------|-------------------|---|
| DMA_IRQ_EN_REG | 0x00 | DMA IRQ Enable Register |
| DMA_IRQ_PEND_REG | 0x10 | DMA IRQ Pending Register |
| DMA_AUTO_GATE_REG | 0x20 | DMA Auto Gating Register |
| DMA_STA_REG | 0x30 | DMA Status Register |
| DMA_EN_REG | 0x100+N*0x40 | DMA Channel Enable Register (N=0~7) |
| DMA_PAU_REG | 0x100+N*0x40+0x4 | DMA Channel Pause Register(N=0~7) |
| DMA_DESC_ADDR_REG | 0x100+N*0x40+0x8 | DMA Channel Start Address Register(N=0~7) |
| DMA_CFG_REG | 0x100+N*0x40+0xC | DMA Channel Configuration Register(N=0~7) |
| DMA_CUR_SRC_REG | 0x100+N*0x40+0x10 | DMA Channel Current Source Register(N=0~7) |
| DMA_CUR_DEST_REG | 0x100+N*0x40+0x14 | DMA Channel Current Destination Register(N=0~7) |
| DMA_BCNT_LEFT_REG | 0x100+N*0x40+0x18 | DMA Channel Byte Counter Left Register(N=0~7) |
| DMA_PARA_REG | 0x100+N*0x40+0x1C | DMA Channel Parameter Register(N=0~7) |

4.8.4. DMA Register Description

4.8.4.1. DMA IRQ Enable Register0 (Default Value: 0x00000000)

| Offset: 0x0000 | | | Register Name: DMA_IRQ_EN_REG0 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30 | R/W | 0x0 | DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 29 | R/W | 0x0 | DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 28 | R/W | 0x0 | DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 27 | / | / | / |
| 26 | R/W | 0x0 | DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 25 | R/W | 0x0 | DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 24 | R/W | 0x0 | DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 23 | / | / | / |

| | | | |
|----|-----|-----|---|
| 22 | R/W | 0x0 | DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 21 | R/W | 0x0 | DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 20 | R/W | 0x0 | DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 19 | / | / | / |
| 18 | R/W | 0x0 | DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 17 | R/W | 0x0 | DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 16 | R/W | 0x0 | DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 15 | / | / | / |
| 14 | R/W | 0x0 | DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 13 | R/W | 0x0 | DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 12 | R/W | 0x0 | DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 11 | / | / | / |
| 10 | R/W | 0x0 | DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 9 | R/W | 0x0 | DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 8 | R/W | 0x0 | DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 7 | / | / | / |
| 6 | R/W | 0x0 | DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 5 | R/W | 0x0 | DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 4 | R/W | 0x0 | DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 3 | / | / | / |
| 2 | R/W | 0x0 | DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 1 | R/W | 0x0 | DMA0_PKG_IRQ_EN |

| | | | |
|---|-----|-----|--|
| | | | DMA 0 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable. |
| 0 | R/W | 0x0 | DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable |

4.8.4.2. DMA IRQ Pending Status Register (Default Value: 0x00000000)

| Offset:0x10 | | | Register Name: DMA_IRQ_PEND_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30 | R/W | 0x0 | DMA7_QUEUE_IRQ_PEND. DMA 7 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 29 | R/W | 0x0 | DMA7_PKG_IRQ_PEND DMA 7 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 28 | R/W | 0x0 | DMA7_HLAF_IRQ_PEND. DMA 7 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 27 | / | / | / |
| 26 | R/W | 0x0 | DMA6_QUEUE_IRQ_PEND. DMA 6 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 25 | R/W | 0x0 | DMA6_PKG_IRQ_PEND DMA 6 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 24 | R/W | 0x0 | DMA6_HLAF_IRQ_PEND. DMA 6 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 23 | / | / | / |
| 22 | R/W | 0x0 | DMA5_QUEUE_IRQ_PEND. DMA 5 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 21 | R/W | 0x0 | DMA5_PKG_IRQ_PEND DMA 5 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 20 | R/W | 0x0 | DMA5_HLAF_IRQ_PEND. DMA 5 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 19 | / | / | / |
| 18 | R/W | 0x0 | DMA4_QUEUE_IRQ_PEND. DMA 4 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 17 | R/W | 0x0 | DMA4_PKG_IRQ_PEND DMA 4 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 16 | R/W | 0x0 | DMA4_HLAF_IRQ_PEND. DMA 4 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 15 | / | / | / |
| 14 | R/W | 0x0 | DMA3_QUEUE_IRQ_PEND. |

| | | | |
|----|-----|-----|--|
| | | | DMA 3 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 13 | R/W | 0x0 | DMA3_PKG_IRQ_PEND DMA 3 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 12 | R/W | 0x0 | DMA3_HLAF_IRQ_PEND. DMA 3 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 11 | / | / | / |
| 10 | R/W | 0x0 | DMA2_QUEUE_IRQ_PEND. DMA 2 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 9 | R/W | 0x0 | DMA2_PKG_IRQ_PEND DMA 2 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 8 | R/W | 0x0 | DMA2_HLAF_IRQ_PEND. DMA 2 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 7 | / | / | / |
| 6 | R/W | 0x0 | DMA1_QUEUE_IRQ_PEND. DMA 1 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 5 | R/W | 0x0 | DMA1_PKG_IRQ_PEND DMA 1 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 4 | R/W | 0x0 | DMA1_HLAF_IRQ_PEND. DMA 1 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 3 | / | / | / |
| 2 | R/W | 0x0 | DMA0_QUEUE_IRQ_PEND. DMA 0 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 1 | R/W | 0x0 | DMA0_PKG_IRQ_PEND DMA 0 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |
| 0 | R/W | 0x0 | DMA0_HLAF_IRQ_PEND. DMA 0 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending. |

4.8.4.3. DMA Auto Gating Register (Default Value: 0x00000000)

| Offset:0x20 | | | Register Name: DMA_AUTO_GATE_REG |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:3 | / | / | / |
| 2 | R/W | 0x0 | DMA_MCLK_CIRCUIT. DMA MCLK interface circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable. |
| 1 | R/W | 0x0 | DMA_COMMON_CIRCUIT. DMA common circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable. |

| | | | |
|---|-----|-----|---|
| 0 | R/W | 0x0 | DMA_CHAN_CIRCUIT. DMA channel circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable. |
|---|-----|-----|---|

Note: When initializing DMA Controller, bit-2 should be set up.

4.8.4.4. DMA Status Register (Default Value: 0x00000000)

| Offset: 0x30 | | | Register Name: DMA_STA_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | RO | 0x0 | DMA7_STATUS DMA Channel 7 Status. 0: Idle 1: Busy |
| 6 | RO | 0x0 | DMA6_STATUS DMA Channel 6 Status. 0: Idle 1: Busy |
| 5 | RO | 0x0 | DMA5_STATUS DMA Channel 5 Status. 0: Idle 1: Busy |
| 4 | RO | 0x0 | DMA4_STATUS DMA Channel 4 Status. 0: Idle 1: Busy. |
| 3 | RO | 0x0 | DMA3_STATUS DMA Channel 3 Status. 0: Idle 1: Busy. |
| 2 | RO | 0x0 | DMA2_STATUS DMA Channel 2 Status. 0: Idle, 1: Busy. |
| 1 | RO | 0x0 | DMA1_STATUS DMA Channel 1 Status. 0: Idle, 1: Busy. |
| 0 | RO | 0x0 | DMA0_STATUS DMA Channel 0 Status. 0: Idle, 1: Busy. |

4.8.4.5. DMA Channel Enable Register (Default Value: 0x00000000)

| Offset: 0x100+N*0x40+0x0(N=0~7) | | | Register Name: DMA_EN_REG |
|---------------------------------|-----|-------------|----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | DMA_EN. DMA Channel Enable |

| | | | |
|--|--|--|--------------------------|
| | | | 0: Disable 1: Enable. |
|--|--|--|--------------------------|

Note:It's not recommended to disable dma while dma is transmitting.If it is necessary to do that,dma has to be paused first and then disabled.

4.8.4.6. DMA Channel Pause Register (Default Value: 0x00000000)

| Offset: 0x100+N*0x40+0x4(N=0~7) | | | Register Name: DMA_PAU_REG |
|---------------------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | DMA_PAUSE. Pausing DMA Channel Transfer Data. 0: Resume Transferring, 1: Pause Transferring. |

4.8.4.7. DMA Channel Descriptor Address Register(Default Value: 0x00000000)

| Offset: 0x100+N*0x40+0x8(N=0~7) | | | Register Name: DMA_DESC_ADDR_REG |
|---------------------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | DMA_DESC_ADDR DMA Channel Descriptor Address. |

4.8.4.8. DMA Channel Configuration Register (Default Value: 0x00000000)

| Offset: 0x100+N*0x40+0xC(N=0~7) | | | Register Name: DMA_CFG_REG |
|---------------------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:27 | / | / | / |
| 26:25 | RO | 0x0 | DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: / |
| 24:23 | RO | 0x0 | DMA_DEST_BST_LEN. DMA Destination Burst Length. 00: 1 01: / 10: 8 11: / |
| 22:21 | RO | 0x0 | DMA_ADDR_MODE. DMA Destination Address Mode 0x0: Linear Mode 0x1: IO Mode 0x2: / 0x3: / |
| 20:16 | RO | 0x0 | DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation. |
| 15:11 | / | / | / |
| 10:9 | RO | 0x0 | DMA_SRC_DATA_WIDTH. |

| | | | |
|-----|----|-----|---|
| | | | DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: / |
| 8:7 | RO | 0x0 | DMA_SRC_BST_LEN. DMA Source Burst Length. 00: 1 01: / 10: 8 11: / |
| 6:5 | RO | 0x0 | DMA_SRC_ADDR_MODE. DMA Source Address Mode 0x0: Linear Mode 0x1: IO Mode 0x2: / 0x3: / |
| 4:0 | RO | 0x0 | DMA_SRC_DRQ_TYPE. DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation. |

Note1: If the DRQ type is dram, then, the corresponding burst length will be fixed, and the options will be invalid.

Note2: The address of the DMA Channel Configuration Register must be word-aligned.

Note3: If the DRQ type is SRAM, then, the source address or destination address must be word-aligned.

4.8.4.9. DMA Channel Current Source Address Register (Default Value: 0x00000000)

| Offset: 0x100+N*0x40+0x10(N=0~7) | | | Register Name: DMA_CUR_SRC_REG |
|----------------------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | RO | 0x0 | DMA_CUR_SRC. DMA Channel Current Source Address, read only. |

Note: The address of the **DMA Channel Current Source Address Register** must be word-aligned.

4.8.4.10. DMA Channel Current Destination Address Register (Default Value: 0x00000000)

| Offset: 0x100+N*0x40+0x14(N=0~7) | | | Register Name: DMA_CUR_DEST_REG |
|----------------------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | RO | 0 | DMA_CUR_DEST. DMA Channel Current Destination Address, read only. |

Note: The address of the **DMA Channel Current Destination Address Register** must be word-aligned.

4.8.4.11. DMA Channel Byte Counter Left Register (Default Value: 0x00000000)

| Offset: 0x100+N*0x40+0x18(N=0~11) | | | Register Name: DMA_BCNT_LEFT_REG |
|-----------------------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:25 | / | / | / |
| 24:0 | RO | 0x0 | DMA_BCNT_LEFT. DMA Channel Byte Counter Left, read only. |

Note: The address of the *DMA Channel Byte Counter Left Register* must be word-aligned.

4.8.4.12. DMA Channel Parameter Register (Default Value: 0x00000000)

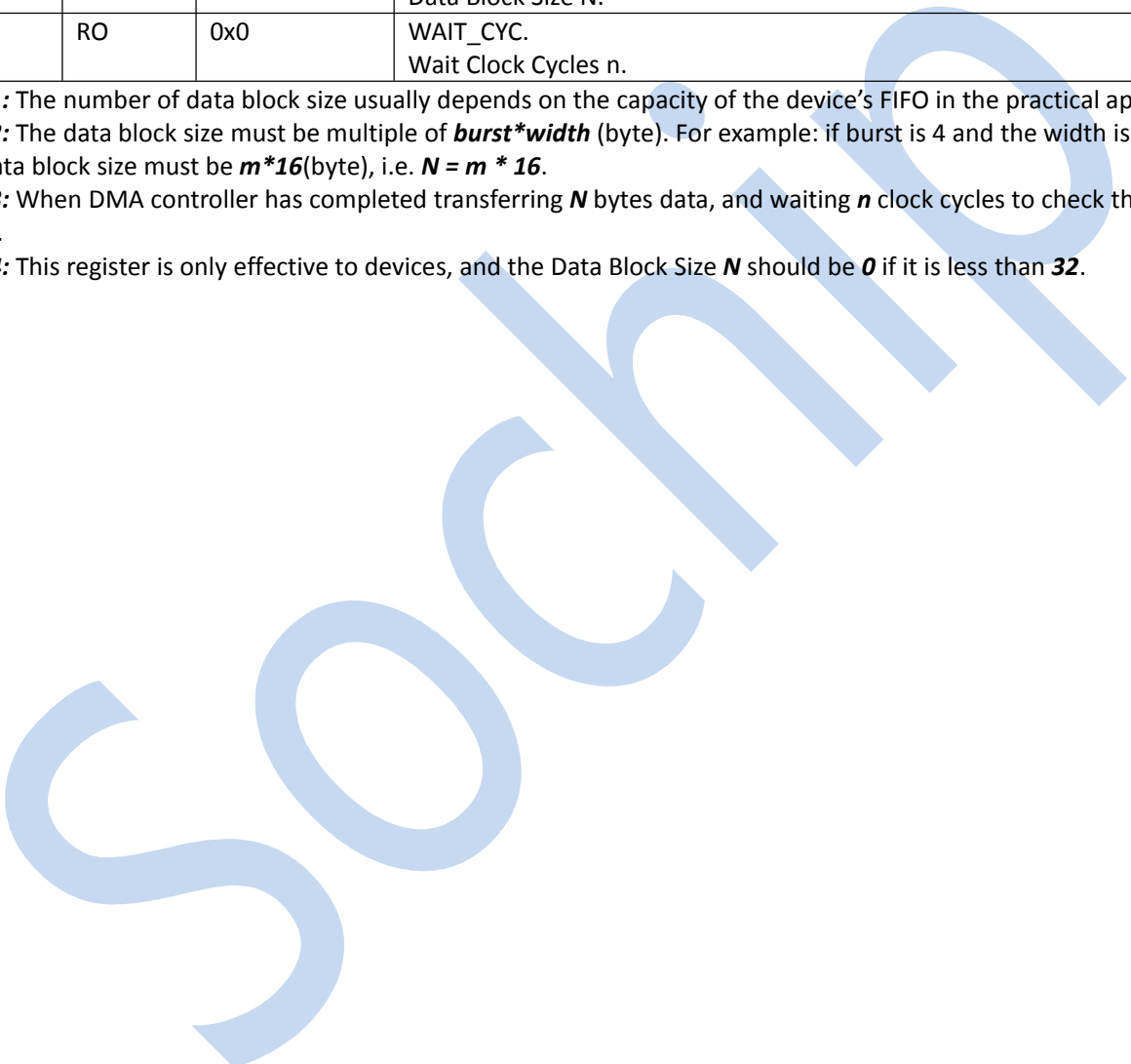
| Offset: 0x100+N*0x40+0x1C(N=0~7) | | | Register Name: DMA_PARA_REG |
|----------------------------------|-----|-------------|--------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:16 | / | / | / |
| 15:8 | RO | 0x0 | DATA_BLK_SIZE. Data Block Size N. |
| 7:0 | RO | 0x0 | WAIT_CYC. Wait Clock Cycles n. |

Note1: The number of data block size usually depends on the capacity of the device's FIFO in the practical application.

Note2: The data block size must be multiple of *burst*width* (byte). For example: if burst is 4 and the width is 32-bit, so the data block size must be $m*16$ (byte), i.e. $N = m * 16$.

Note3: When DMA controller has completed transferring *N* bytes data, and waiting *n* clock cycles to check the DRQ signal.

Note4: This register is only effective to devices, and the Data Block Size *N* should be **0** if it is less than **32**.



4.9. GIC

For details about GIC, please refer to the *GIC PL400 technical reference manual* and *ARM GIC Architecture Specification V2.0*.

4.9.1. Interrupt Source

| Interrupt number | Vector | Interrupt Source | Description |
|------------------|--------|------------------|------------------|
| 0 | 0x0000 | SGI 0 | SGI 0 interrupt |
| 1 | 0x0004 | SGI 1 | SGI 1 interrupt |
| 2 | 0x0008 | SGI 2 | SGI 2 interrupt |
| 3 | 0x000C | SGI 3 | SGI 3 interrupt |
| 4 | 0x0010 | SGI 4 | SGI 4 interrupt |
| 5 | 0x0014 | SGI 5 | SGI 5 interrupt |
| 6 | 0x0018 | SGI 6 | SGI 6 interrupt |
| 7 | 0x001C | SGI 7 | SGI 7 interrupt |
| 8 | 0x0020 | SGI 8 | SGI 8 interrupt |
| 9 | 0x0024 | SGI 9 | SGI 9 interrupt |
| 10 | 0x0028 | SGI 10 | SGI 10 interrupt |
| 11 | 0x002C | SGI 11 | SGI 11 interrupt |
| 12 | 0x0030 | SGI 12 | SGI 12 interrupt |
| 13 | 0x0034 | SGI 13 | SGI 13 interrupt |
| 14 | 0x0038 | SGI 14 | SGI 14 interrupt |
| 15 | 0x003C | SGI 15 | SGI 15 interrupt |
| 16 | 0x0040 | PPI 0 | PPI 0 interrupt |
| 17 | 0x0044 | PPI 1 | PPI 1 interrupt |
| 18 | 0x0048 | PPI 2 | PPI 2 interrupt |
| 19 | 0x004C | PPI 3 | PPI 3 interrupt |
| 20 | 0x0050 | PPI 4 | PPI 4 interrupt |
| 21 | 0x0054 | PPI 5 | PPI 5 interrupt |
| 22 | 0x0058 | PPI 6 | PPI 6 interrupt |
| 23 | 0x005C | PPI 7 | PPI 7 interrupt |
| 24 | 0x0060 | PPI 8 | PPI 8 interrupt |
| 25 | 0x0064 | PPI 9 | PPI 9 interrupt |
| 26 | 0x0068 | PPI 10 | PPI 10 interrupt |
| 27 | 0x006C | PPI 11 | PPI 11 interrupt |
| 28 | 0x0070 | PPI 12 | PPI 12 interrupt |
| 29 | 0x0074 | PPI 13 | PPI 13 interrupt |
| 30 | 0x0078 | PPI 14 | PPI 14 interrupt |
| 31 | 0x007C | PPI 15 | PPI 15 interrupt |
| 32 | 0x0080 | UART 0 | UART 0 interrupt |
| 33 | 0x0084 | UART 1 | UART 1 interrupt |
| 34 | 0x0088 | UART 2 | UART 2 interrupt |
| 35 | 0x008C | | |
| 36 | 0x0090 | | |
| 37 | 0x0094 | | |
| 38 | 0x0098 | TWI 0 | TWI 0 interrupt |
| 39 | 0x009C | TWI 1 | TWI 1 interrupt |
| 40 | 0x00A0 | | |
| 41 | 0x00A4 | | |
| 42 | 0x00A8 | | |

| | | | |
|----|--------|--------------|------------------------------------|
| 43 | 0x00AC | | |
| 44 | 0x00B0 | | |
| 45 | 0x00B4 | I2S/PCM | I2S/PCM interrupt |
| 46 | 0x00B8 | | |
| 47 | 0x00BC | PB_EINT | PB_EINT interrupt |
| 48 | 0x00C0 | | |
| 49 | 0x00C4 | PG_EINT | PG_EINT interrupt |
| 50 | 0x00C8 | Timer 0 | Timer 0 interrupt |
| 51 | 0x00CC | Timer 1 | Timer 1 interrupt |
| 52 | 0x00D0 | Timer 2 | Timer 2 interrupt |
| 53 | 0x00D4 | | |
| 54 | 0x00D8 | | |
| 55 | 0x00DC | | |
| 56 | 0x00E0 | | |
| 57 | 0x00E4 | Watchdog | Watchdog interrupt |
| 58 | 0x00E8 | | |
| 59 | 0x00EC | | |
| 60 | 0x00F0 | | |
| 61 | 0x00F4 | Audio Codec | Audio Codec interrupt |
| 62 | 0x00F8 | LRADC | LRADC interrupt |
| 63 | 0x00FC | | |
| 64 | 0x100 | External NMI | External Non-Mask Interrupt |
| 65 | 0x104 | | |
| 66 | 0x108 | | |
| 67 | 0x010C | | |
| 68 | 0x0110 | | |
| 69 | 0x0114 | | |
| 70 | 0x0118 | | |
| 71 | 0x011C | | |
| 72 | 0x0120 | Alarm 0 | Alarm 0 interrupt |
| 73 | 0x0124 | Alarm 1 | Alarm 1 interrupt |
| 74 | 0x0128 | | |
| 75 | 0x012C | | |
| 76 | 0x0130 | | |
| 77 | 0x0134 | | |
| 78 | 0x0138 | | |
| 79 | 0x013C | | |
| 80 | 0x0140 | | |
| 81 | 0x0144 | | |
| 82 | 0x0148 | DMA | DMA channel interrupt |
| 83 | 0x014C | HS Timer0 | HS Timer0 interrupt |
| 84 | 0x0150 | HS Timer1 | HS Timer1 interrupt |
| 85 | 0x0154 | | |
| 86 | 0x0158 | | |
| 87 | 0x015C | | |
| 88 | 0x0160 | | |
| 89 | 0x0164 | | |
| 90 | 0x0168 | VE | VE interrupt |
| 91 | 0x016C | | |
| 92 | 0x0170 | SD/MMC 0 | SD/MMC Host Controller 0 interrupt |
| 93 | 0x0174 | SD/MMC 1 | SD/MMC Host Controller 1 interrupt |
| 94 | 0x0178 | SD/MMC 2 | SD/MMC Host Controller 2 interrupt |
| 95 | 0x017C | | |

| | | | |
|-----|--------|----------------|---------------------------|
| 96 | 0x0180 | | |
| 97 | 0x0184 | SPI | SPI interrupt |
| 98 | 0x0188 | | |
| 99 | 0x018C | | |
| 100 | 0x0190 | | |
| 101 | 0x0194 | | |
| 102 | 0x0198 | | |
| 103 | 0x019C | USB OTG_Device | USB OTG_Device interrupt |
| 104 | 0x01A0 | USB OTG_EHCI | USB OTG_EHCI I interrupt |
| 105 | 0x01A4 | USB OTG_OHCI | USB OTG_OHCI interrupt |
| 106 | 0x01A8 | | |
| 107 | 0x01AC | | |
| 108 | 0x01B0 | | |
| 109 | 0x01B4 | | |
| 110 | 0x01B8 | | |
| 111 | 0x01BC | | |
| 112 | 0x01C0 | CE | CE interrupt |
| 113 | 0x01C4 | | |
| 114 | 0x01C8 | EMAC | EMAC interrupt |
| 115 | 0x01CC | CSI0 | CSI0 interrupt |
| 116 | 0x01D0 | CSI1 | CSI1 interrupt |
| 117 | 0x01D4 | CSI_CCI | CSI_CCI interrupt |
| 118 | 0x01D8 | TCON | TCON Controller interrupt |
| 119 | 0x01DC | | |
| 120 | 0x01E0 | | |
| 121 | 0x01E4 | | |
| 122 | 0x01E8 | MIPI CSI | MIPI CSI interrupt |
| 123 | 0x01EC | | |
| 124 | 0x01F0 | | |
| 125 | 0x01F4 | | |
| 126 | 0x01F8 | | |
| 127 | 0x01FC | DE | DE interrupt |
| 128 | 0x0200 | | |
| 129 | 0x0204 | | |
| 130 | 0x0208 | | |
| 131 | 0x020C | | |
| 132 | 0x0210 | | |
| 133 | 0x0214 | | |
| 134 | 0x0218 | | |
| 135 | 0x021C | | |
| 136 | 0x0220 | | |
| 137 | 0x0224 | | |
| 138 | 0x0228 | | |
| 139 | 0x022C | | |
| 140 | 0x0230 | CTI0 | CTI0 interrupt |
| 141 | 0x0234 | CTI1 | CTI1 interrupt |
| 142 | 0x0238 | CTI2 | CTI2 interrupt |
| 143 | 0x023C | CTI3 | CTI3 interrupt |
| 144 | 0x0240 | COMMTX0 | COMMTX0 interrupt |
| 145 | 0x0244 | COMMTX1 | COMMTX1 interrupt |
| 146 | 0x0248 | COMMTX2 | COMMTX2 interrupt |
| 147 | 0x024C | COMMTX3 | COMMTX3 interrupt |
| 148 | 0x0250 | COMMRX0 | COMMRX0 interrupt |

| | | | |
|-----|--------|-----------|---------------------|
| 159 | 0x0254 | COMMRX1 | COMMRX1 interrupt |
| 150 | 0x0258 | COMMRX2 | COMMRX2 interrupt |
| 151 | 0x025C | COMMRX3 | COMMRX3 interrupt |
| 152 | 0x0260 | PMU0 | PMU0 interrupt |
| 153 | 0x0264 | PMU1 | PMU1 interrupt |
| 154 | 0x0268 | PMU2 | PMU2 interrupt |
| 155 | 0x026C | PMU3 | PMU3 interrupt |
| 156 | 0x0270 | AXI_ERROR | AXI_ERROR interrupt |
| | | | |

4.10. Crypto Engine

4.10.1. Overview

The Crypto Engine (CE) is one encrypt/ decrypt function accelerator. It is suitable for a variety of applications. It can support encryption/decryption and calculate the hash value. Besides, both CPU mode and DMA method are supported for different applications.

It includes the following features:

- Support AES, DES, 3DES, SHA-1, MD5
- 160-bits hardware PRNG with 175-bits seed
- Support ECB, CBC, CTR, CTS modes for AES
- Support ECB, CBC, CTR modes for DES/3DES
- 128-bits, 192-bits and 256-bits key size for AES
- Support 32-words RX FIFO and 32-words TX FIFO for high speed application
- Support CPU mode and DMA mode

4.10.2. Block Diagram

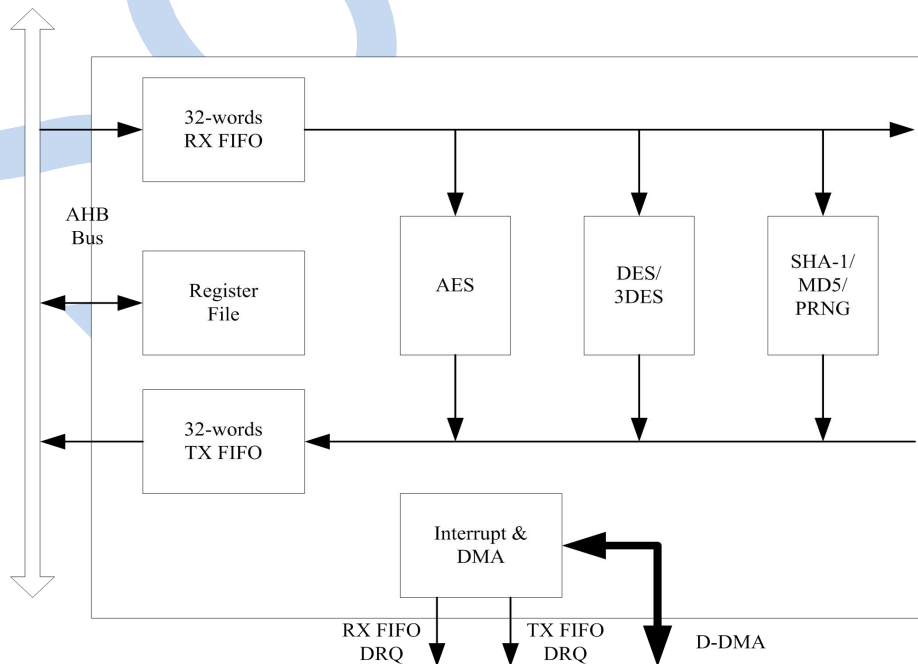


Figure 4-7. CE Block Diagram

4.10.3. Crypto Engine Register List

| Module Name | Base Address |
|-------------|--------------|
| CE | 0x01C15000 |

| Register Name | Offset | Description |
|---------------|--------|--------------------------------------|
| CE_CTL | 0x00 | Control Register |
| CE_KEY0 | 0x04 | Input Key 0/ PRNG Seed 0 |
| CE_KEY1 | 0x08 | Input Key 1/ PRNG Seed 1 |
| ... | ... | ... |
| CE_KEY7 | 0x20 | Input Key 7 |
| CE_IV0 | 0x24 | Initialization Vector 0 |
| CE_IV1 | 0x28 | Initialization Vector 1 |
| CE_IV2 | 0x2C | Initialization Vector 2 |
| CE_IV3 | 0x30 | Initialization Vector 3 |
| CE_CNT0 | 0x34 | Preload Counter 0 |
| CE_CNT1 | 0x38 | Preload Counter 1 |
| CE_CNT2 | 0x3C | Preload Counter 2 |
| CE_CNT3 | 0x40 | Preload Counter 3 |
| CE_FCSR | 0x44 | FIFO Control/ Status Register |
| CE_ICSR | 0x48 | Interrupt Control/ Status Register |
| CE_MD0 | 0x4C | SHA1/MD5 Message Digest 0/PRNG Data0 |
| CE_MD1 | 0x50 | SHA1/MD5 Message Digest 1/PRNG Data1 |
| CE_MD2 | 0x54 | SHA1/MD5 Message Digest 2/PRNG Data2 |
| CE_MD3 | 0x58 | SHA1/MD5 Message Digest 3/PRNG Data3 |
| CE_MD4 | 0x5C | SHA1/MD5 Message Digest 4/PRNG Data4 |
| CE_CTS_LEN | 0x60 | AES-CTS ciphertext length |
| CE_RXFIFO | 0x200 | RX FIFO input port |
| CE_TXFIFO | 0x204 | TX FIFO output port |

4.10.4. Crypto Engine Register Description

4.10.4.1. Control Register(Default Value: 0x00000000)

| Offset: 0x00 | | | Register Name: CE_CTL |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| 27:24 | R/W | 0 | SKEY_SELECT AES/DES/3DES key select 0: Select input CE_KEYx (Normal Mode) 1: / 2: / |

| | | | |
|-------|-----|---|---|
| | | | 3-10: Select internal Key n (n from 0 to 7) Others: Reserved |
| 18:16 | R | x | DIE_ID Die Bonding ID |
| 15 | R/W | 0 | PRNG_MODE PRNG generator mode 0: One-shot mode 1: Continue mode |
| 14 | R/W | 0 | IV_MODE IV Steady of SHA-1/MD5 constants 0: Constants 1: Arbitrary IV Notes: It is only used for SHA-1/MD5 engine. If the number of IV word is beyond of 4, Counter 0 register is used for IV4. |
| 13:12 | R/W | 0 | CE_OP_MODE CE Operation Mode 00: Electronic Code Book (ECB) mode 01: Cipher Block Chaining (CBC) mode 10:Counter (CTR) mode 11: AES Ciphertext Stealing (CTS) mode |
| 11:10 | / | / | / |
| 9:8 | R/W | 0 | AES_KEY_SIZE Key Size for AES 00: 128-bits 01: 192-bits 10: 256-bits 11: Reserved |
| 7 | R/W | 0 | CE_OP_DIR CE Operation Direction 0: Encryption 1: Decryption |
| 6:4 | R/W | 0 | CE_METHOD CE Method 000: AES 001: DES 010: Triple DES (3DES) 011: SHA-1 100: MD5 101: PRNG Others: Reserved |
| 3 | / | / | / |
| 2 | R/W | 0 | SHA1_MD5_END_BIT SHA-1/MD5 Data End bit Write '1' to tell SHA-1/MD5 engine that the text data is end. If there is some data in FIFO, the engine would fetch these data and process them. After finishing message digest, this bit is clear to '0' by hardware and message digest can be read out from digest registers. Notes: It is only used for SHA-1/MD5 engine. |
| 1 | R/W | 0 | PRNG_START PRNG start bit In PRNG one-shot mode, write '1' to start PRNG. After generating one group random data (5 words), this bit is clear to '0' by hardware. |
| 0 | R/W | 0 | CE_ENABLE CE Enable |

| | | | |
|--|--|--|---|
| | | | A disable on this bit overrides any other block and flushes all FIFOs. 0: Disable 1: Enable |
|--|--|--|---|

4.10.4.2. Key [n] Register (Default Value: 0x00000000)

| Offset: 0x04+4*n | | | Register Name: CE_KEY[n] |
|------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | CE_KEY Key[n] Input Value (n= 0~7)/ PRNG Seed[n] (n= 0~5) |

4.10.4.3. IV[n] Register(Default Value: 0x00000000)

| Offset: 0x24+4*n | | | Register Name: CE_IV[n] |
|------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | CE_IV_VALUE Initialization Vector (IV[n]) Input Value (n= 0~3) |

4.10.4.4. Count [n] Register (Default Value: 0x00000000)

| Offset: 0x34+4*n | | | Register Name: CE_CNT[n] |
|------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | CE_CNT_VALUE Counter Input Value (n= 0~3) |

4.10.4.5. FIFO Control/ Status Register (Default Value: 0x60000F0F)

| Offset: 0x44 | | | Register Name: CE_FCSR |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30 | R | 0x1 | RXFIFO_STATUS RX FIFO Empty 0: No room for new word in RX FIFO 1: More than one room for new word in RX FIFO (>= 1 word) |
| 29:24 | R | 0x20 | RXFIFO_EMP_CNT RX FIFO Empty Space Word Counter |
| 23 | / | / | / |
| 22 | R | 0 | TXFIFO_STATUS TX FIFO Data Available Flag 0: No available data in TX FIFO 1: More than one data in TX FIFO (>= 1 word) |
| 21:16 | R | 0 | TXFIFO_AVA_CNT TX FIFO Available Word Counter |
| 15:13 | / | / | / |
| 12:8 | R/W | 0xF | RXFIFO_INT_TRIG_LEVEL RX FIFO Empty Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition |

| | | | |
|-----|-----|-----|---|
| | | | Trigger Level = RXTL + 1 Notes: RX FIFO is used for input the data. |
| 7:5 | / | / | / |
| 4:0 | R/W | 0xF | TXFIFO_INT_TRIG_LEVEL TX FIFO Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL + 1 Notes: TX FIFO is used for output the result data. |

4.10.4.6. Interrupt Control/ Status Register (Default Value: 0x00000000)

| Offset: 0x48 | | | Register Name: CE_ICSR |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:11 | / | / | / |
| 10 | R/W | 0 | RXFIFO_EMP_PENDING_BIT RX FIFO Empty Pending bit 0: No pending 1: RX FIFO Empty pending Notes: Write '1' to clear or automatic clear if interrupt condition fails. |
| 9 | / | / | / |
| 8 | R/W | 0 | TXFIFO_AVA_PENDING_BIT TX FIFO Data Available Pending bit 0: No TX FIFO pending 1: TX FIFO pending Notes: Write '1' to clear or automatic clear if interrupt condition fails. |
| 7:5 | / | / | / |
| 4 | R/W | 0 | DRA_ENABLE DRQ Enable 0: Disable DRQ (CPU polling mode) 1: Enable DRQ (DMA mode) |
| 3 | / | / | / |
| 2 | R/W | 0 | RXFIFO_EMP_INT_ENABLE RX FIFO Empty Interrupt Enable 0: Disable 1: Enable Notes: If it is set to '1', when the number of empty room is great or equal (>=) the preset threshold, the interrupt is trigger and the correspond flag is set. |
| 1 | / | / | / |
| 0 | R/W | 0 | TXFIFO_AVA_INT_ENABLE TX FIFO Data Available Interrupt Enable 0: Disable 1: Enable Notes: If it is set to '1', when available data number is great or equal (>=) the preset threshold, the interrupt is trigger and the correspond flag is set. |

4.10.4.7. Message Digest[n] Register (Default Value: 0x00000000)

| Offset: 0x4C+4*n | | | Register Name: CE_MD[n] |
|------------------|-----|-------------|-------------------------|
| Bit | R/W | Default/Hex | Description |

| | | | |
|------|---|---|---|
| 31:0 | R | 0 | CE_MID_DATA SHA1/ MD5 Message digest MD[n] for SHA1/MD5 (n= 0~4) |
|------|---|---|---|

4.10.4.8. CTS Length Register (Default Value: 0x00000000)

| | | | |
|--------------|-----|-------------|---|
| Offset: 0x60 | | | Register Name: CE_CTS_LEN |
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | AES-CTS ciphertext length in byte unit The value of '0' means no data. |

4.10.4.9. RXFIFO Register (Default Value: 0x00000000)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x200 | | | Register Name: CE_RX |
| Bit | R/W | Default/Hex | Description |
| 31:0 | W | 0 | CE_RX_FIFO 32-bits RX FIFO for Input |

4.10.4.10. TXFIFO Register (Default Value: 0x00000000)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x204 | | | Register Name: CE_TX |
| Bit | R/W | Default/Hex | Description |
| 31:0 | W | 0 | CE_TX_FIFO 32-bits TX FIFO for Output |

4.10.5. Crypto Engine Clock Requirement

| Clock Name | Description | Requirement |
|------------|----------------------------|-------------|
| ahb_clk | AHB bus clock | >=24MHz |
| CE_clk | Crypto Engine serial clock | <= 150MHz |

4.10.6. Crypto Engine Programming Guide

- (1) AES CTS can only support oneshot mode that all sources are writing in the RXFIFO as a package. AES CTS can not support continue sub-package mode that the sources could divide into some packages to calculate.
- (2) For SHA1, it should be noted the sequence of the initial hash value.

SHA1 is the big-endian algorithm, within each word, the most significant bit is stored in the left-most bit position. For example, the initial hash value of SHA1 in Fips180-2, $H^{(0)}$ shall consist of the following five 32-bit words, in hex:

$H_0^{(0)} = 67452301$

$H_1^{(0)} = \text{efcdab89}$

$H_2^{(0)} = 98badcfe$

$H_3^{(0)} = 10325476$

$H_4^{(0)} = \text{c3d2e1f0}$

The default access mode of ARM is little-endian. So for the SHA1 of the Sochip, the initial hash value, writing in the CE_IV[0]、CE_IV[1]、CE_IV[2]、CE_IV[3]、CE_CNT[0], in hex:

CE_IV[0] = 01234567

CE_IV[1] = 89abcdef

CE_IV[2] = fedcba98
CE_IV[3] = 76543210
CE_CNT[0] = f0e1d2c3

Sochip

4.11. Security ID

4.11.1. Overview

There is one on chip EFUSE, with size up to 128bits for security chip ID, the other 128bits is reserved. The work clock of Security ID is 6MHz.

Sochip

4.12. LRADC

4.12.1. Overview

The LRADC is 6-bit resolution ADC for key application. The LRADC can work up to 250Hz conversion rate.

The LRADC includes the following features:

- Supports APB 32-bits bus width
- Support interrupt
- Support Hold Key and General Key
- Support Single Key and Continue Key mode
- 6-bits resolution
- Voltage input range between 0V to 2.0V
- Sample rate up to 250Hz

4.12.2. Clock Source

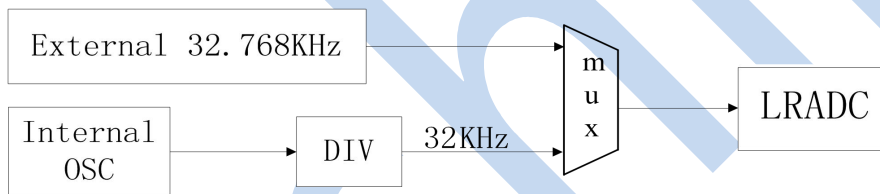


Figure 4-8. LRADC Clock Source

4.12.3. Operation Principle

The LRADC converted data can accessed by interrupt and polling method. If software can't access the last converted data instantly, the new converted data would update the old one at new sampling data.

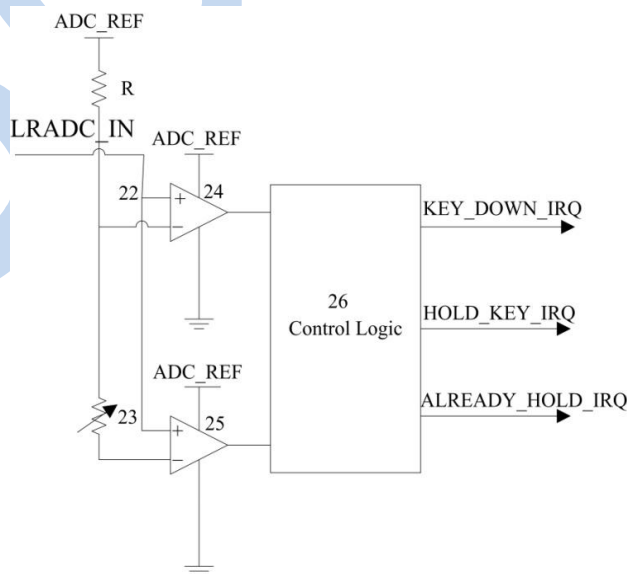


Figure 4-9. LRADC Data Converted Diagram

When ADC_IN Signal change from 3.0V to less than 2.0V (Level A), the comparator24 send first interrupt to control logic; When ADC_IN Signal change from 2.0V to less than certain level (Program can set), the comparator25 give second interrupt. If the control Logic get the first interrupt, In a certain time range (program can set), doesn't get second interrupt, it will send hold key interrupt to the host; If the control Logic get the first interrupt, In a certain time range (program can set), get second interrupt, it will send key down interrupt to the host; If the control logic only get the second interrupt, doesn't get the first interrupt, it will send already hold interrupt to the host.

The LRADC have three mode, Normal Mode、Single Mode and Continue Mode. Normal mode is that the LRADC will report the result data of each convert all the time when the key is down. Single Mode is that the LRADC will only report the first convert result data when the key is down. Continue Mode is that the LRADC will report one of 8*(N+1) (N is program can set) sample convert result data when key is down.

The LRADC is support four sample rate such as 250Hz、125Hz、62.5Hz and 32.25Hz, you can configure the value of LRADC_SAMPLE_RATE to select the fit sample rate.

4.12.4. LRADC Register List

| Module Name | Base Address |
|-------------|--------------|
| LRADC | 0x01C22800 |

| Register Name | Offset | Description |
|---------------|--------|----------------------------------|
| LRADC_CTRL | 0x00 | LRADC Control Register |
| LRADC_INTC | 0x04 | LRADC Interrupt Control Register |
| LRADC_INTS | 0x08 | LRADC Interrupt Status Register |
| LRADC_DATA0 | 0x0C | LRADC Data0 Register |
| LRADC_DATA1 | 0x10 | LRADC Data1 Register |

4.12.5. LRADC Register Description

4.12.5.1. LRADC Control Register (Default Value: 0x01000168)

| Offset: 0x00 | | | Register Name: LRADC_CTRL_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31: 24 | R/W | 0x1 | FIRST_CONVERT_DLY ADC First Convert Delay setting, ADC conversion is delayed by n samples |
| 23:22 | R/W | 0x0 | ADC_CHAN_SELECT ADC channel select 00: ADC0 channel 01: ADC1 channel 1x: ADC0&ADC1 channel |
| 21:20 | / | / | / |
| 19:16 | R/W | 0x0 | CONTINUE_TIME_SELECT Continue Mode time select, one of 8*(N+1) sample as a valuable sample data |
| 15:14 | / | / | / |
| 13:12 | R/W | 0x0 | KEY_MODE_SELECT Key Mode Select 00: Normal Mode 01: Single Mode 10: Continue Mode |
| 11:8 | R/W | 0x1 | LEVELA_B_CNT |

| | | | |
|------|-----|-----|---|
| | | | Level A to Level B time threshold select, judge ADC convert value in level A to level B in n+1 samples |
| 7 | R/W | 0x0 | LRADC_HOLD_KEY_EN LRADC Hold Key Enable 0: Disable 1: Enable |
| 6 | R/W | 0x1 | LRADC_HOLD_EN LRADC Sample hold Enable 0: Disable 1: Enable |
| 5:4 | R/W | 0x2 | LEVELB_VOL Level B Corresponding Data Value Setting (the real voltage value) 00: 0x3C (~1.9V) 01: 0x39 (~1.8V) 10: 0x36 (~1.7V) 11: 0x33 (~1.6V) |
| 3: 2 | R/W | 0x2 | LRADC_SAMPLE_RATE LRADC Sample Rate 00: 250 Hz 01: 125 Hz 10: 62.5 Hz 11: 32.25 Hz |
| 1 | / | / | / |
| 0 | R/W | 0x0 | LRADC_EN LRADC enable 0: Disable 1: Enable |

4.12.5.2. LRADC Interrupt Control Register (Default Value: 0x00000000)

| Offset: 0x04 | | | Register Name: LRADC_INTC_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:13 | / | / | / |
| 12 | R/W | 0x0 | ADC1_KEYUP_IRQ_EN ADC 1 Key Up IRQ Enable 0: Disable 1: Enable |
| 11 | R/W | 0x0 | ADC1_ALRDY_HOLD_IRQ_EN ADC 1 Already Hold Key IRQ Enable 0: Disable 1: Enable |
| 10 | R/W | 0x0 | ADC1_HOLD_KEY_IRQ_EN ADC 1 Hold Key IRQ Enable 0: Disable 1: Enable |
| 9 | R/W | 0x0 | ADC1_KEYIRQ_EN ADC 1 Key IRQ Enable 0: Disable 1: Enable |
| 8 | R/W | 0x0 | ADC1_DATA_IRQ_EN ADC 1 DATA IRQ Enable 0: Disable 1: Enable |

| | | | |
|-----|-----|-----|---|
| 7:5 | / | / | / |
| 4 | R/W | 0x0 | ADC0_KEYUP_IRQ_EN ADC0 Key Up IRQ Enable 0: Disable 1: Enable |
| 3 | R/W | 0x0 | ADC0_ALRDY_HOLD_IRQ_EN ADC0 Already Hold IRQ Enable 0: Disable 1: Enable |
| 2 | R/W | 0x0 | ADC0_HOLD_IRQ_EN ADC0 Hold Key IRQ Enable 0: Disable 1: Enable |
| 1 | R/W | 0x0 | ADC0_KEYDOWN_EN ADC0 Key Down Enable 0: Disable 1: Enable |
| 0 | R/W | 0x0 | ADC0_DATA_IRQ_EN ADC0 Data IRQ Enable 0: Disable 1: Enable |

4.12.5.3. LRADC Interrupt Status Register (Default Value: 0x00000000)

| Offset: 0x08 | | | Register Name: LRADC_INTS_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:13 | / | / | / |
| 12 | R/W | 0x0 | ADC1_KEYUP_PENDING ADC 1 Key up Pending Bit When general key pull up, it the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable |
| 11 | R/W | 0x0 | ADC1_ALRDY_HOLD_PENDING ADC 1 Already Hold Pending Bit When hold key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable |
| 10 | R/W | 0x0 | ADC1_HOLDKEY_PENDING ADC 1 Hold Key Pending Bit When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable. |
| 9 | R/W | 0x0 | ADC1_KEYDOWN_IRQ_PENDING ADC 1 Key Down IRQ Pending Bit When General key pull down, the status bit is set and the interrupt line is |

| | | | |
|-----|-----|-----|---|
| | | | <p>set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.</p> |
| 8 | R/W | 0x0 | <p>ADC1_DATA_IRQ_PENDING ADC 1 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.</p> |
| 7:5 | / | / | / |
| 4 | R/W | 0x0 | <p>ADC0_KEYUP_PENDING ADC0 Key up Pending Bit When general key pull up, it the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable</p> |
| 3 | R/W | 0x0 | <p>ADC0_ALRDY_HOLD_PENDING ADC0 Already Hold Pending Bit When hold key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable</p> |
| 2 | R/W | 0x0 | <p>ADC0_HOLDKEY_PENDING ADC0 Hold Key Pending Bit When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.</p> |
| 1 | R/W | 0x0 | <p>ADC0_KEYDOWN_PENDING ADC0 Key Down IRQ Pending Bit When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.</p> |
| 0 | R/W | 0x0 | <p>ADC0_DATA_PENDING ADC0 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.</p> |

4.12.5.4. LRADC Data0 Register (Default Value: 0x00000000)

| | |
|--------------|--------------------------------|
| Offset: 0x0C | Register Name: LRADC_DATA0_REG |
|--------------|--------------------------------|

| Bit | R/W | Default/Hex | Description |
|------|-----|-------------|----------------------------|
| 31:6 | / | / | / |
| 5:0 | R | 0x0 | LRADC_DATA0 LRADC Data0 |

4.12.5.5. LRADC Data1 Register (Default Value: 0x00000000)

| Offset: 0x10 | | | Register Name: LRADC_DATA1_REG |
|--------------|-----|-------------|--------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:6 | / | / | / |
| 5:0 | R | 0x0 | LRADC_DATA1 LRADC Data1 |

4.13. RTC

4.13.1. Overview

The real time clock (RTC) is for calendar usage. It is built around a 30-bit counter and used to count elapsed time in YY-MM-DD and HH-MM-SS. The unit can be operated by the backup battery while the system power is off. It has a built-in leap year generator and a independent power pin (RTC_VIO).

The alarm generates an alarm signal at a specified time in the power-off mode or normal operation mode. In normal operation mode, both the alarm interrupt and the power management wakeup are activated. In power-off mode, the power management wakeup signal is activated. In this section, there are two kinds of alarm. Alarm 0 is a general alarm, its counter is based on second. Alarm 1 is a weekly alarm, its counter is based on the real time.

The 32768Hz oscillator is used only to provide a low power, accurate reference for the RTC.

General Purpose Register can be flag register, and it will save the value all the time when the VDD_RTC is not power off.

4.13.2. RTC Register List

| Module Name | Base Address |
|-------------|--------------|
| RTC | 0x01c20400 |

| Register Name | Offset | Description |
|-----------------------|---------------|--|
| LOSC_CTRL_REG | 0x0 | Low Oscillator Control Register |
| LOSC_AUTO_SWT_STA_REG | 0x4 | LOSC Auto Switch Status Register |
| RTC_YY_MM_DD_REG | 0x10 | RTC Year-Month-Day Register |
| RTC_HH_MM_SS_REG | 0x14 | RTC Hour-Minute-Second Register |
| ALARM0_COUNTER_REG | 0x20 | Alarm 0 Counter Register |
| ALARM0_CUR_VLU_REG | 0x24 | Alarm 0 Counter Current Value Register |
| ALARM0_ENABLE_REG | 0x28 | Alarm 0 Enable Register |
| ALARM0_IRQ_EN | 0x2C | Alarm 0 IRQ Enable Register |
| ALARM0_IRQ_STA_REG | 0x30 | Alarm 0 IRQ Status Register |
| ALARM1_WK_HH_MM-SS | 0x40 | Alarm 1 Week HMS Register |
| ALARM1_ENABLE_REG | 0x44 | Alarm 1 Enable Register |
| ALARM1_IRQ_EN | 0x48 | Alarm 1 IRQ Enable Register |
| ALARM1_IRQ_STA_REG | 0x4C | Alarm 1 IRQ Status Register |
| ALARM_CONFIG_REG | 0x50 | Alarm Config Register |
| LOSC_OUT_GATING_REG | 0x60 | LOSC output gating register |
| GP_DATA_REG | 0x100 + N*0x4 | General Purpose Register (N=0~7) |
| VDD_RTC_REG | 0x190 | VDD RTC Regulate Register |
| IC_CHARA_REG | 0x1F0 | IC Characteristic Register |

4.13.3. RTC Register Description

4.13.3.1. LOSC Control Register (Default Value: 0x00004000)

| Offset: 0x00 | | | Register Name: LOSC_CTRL_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | W | 0x0 | KEY_FIELD. Key Field. This field should be filled with 0x16AA, and then the bit 0 can be written with the new value. |
| 15 | / | / | / |
| 14 | R/W | 0x1 | LOSC_AUTO_SWT_EN. LOSC auto switch enable. 0: Disable, 1: Enable. |
| 13:10 | / | / | / |
| 9 | R/W | 0x0 | ALM_DDHHMMSS_ACCE. ALARM DD-HH-MM-SS access. After writing the ALARM DD-HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished. |
| 8 | R/W | 0x0 | RTC_HHMMSS_ACCE. RTC HH-MM-SS access. After writing the RTC HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD register, the YY-MM-DD register will be refreshed for at most one second. |
| 7 | R/W | 0x0 | RTC_YYMMDD_ACCE. RTC YY-MM-DD access. After writing the RTC YY-MM-DD register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD register, the YY-MM-DD register will be refreshed for at most one second. |
| 6:4 | / | / | / |
| 3:2 | R/W | 0x0 | EXT_LOSC_GSM. External 32768Hz Crystal GSM. 00 low 01 10 11 high |
| 1 | / | / | / |
| 0 | R/W | 0x0 | LOSC_SRC_SEL. LOSC Clock source Select. 'N' is the value of Internal OSC Clock Prescaler register. 0: Internal 32KHz, 1: External 32.768KHz OSC. Note: Internal 32KHz is divided from OSC24MHz. |

Note1: Any bit of [9:7] is set, the RTC HH-MM-SS, YY-MM-DD and ALARM DD-HH-MM-SS register can't be written .

4.13.3.2. LOSC Auto Swith Status Register (Default Value: 0x00000000)

| Offset: 0x04 | | | Register Name: LOSC_AUTO_SWT_STA_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:2 | / | / | / |

| | | | |
|---|-----|-----|--|
| 1 | R/W | 0x0 | LOSC_AUTO_SWT_PEND. LOSC auto switch pending. 0: No effect 1: Auto switches pending Set 1 to this bit will clear it. |
| 0 | RO | 0x0 | LOSC_SRC_SEL_STA. Checking LOSC Clock Source Status. 'N' is the value of Internal OSC Clock Prescaler register. 0: Internal 32KHz 1: External 32.768KHz OSC |

4.13.3.3. RTC YY-MM-DD Register (Default Value: 0x00000000)

| Offset: 0x10 | | | Register Name: RTC_YY_MM_DD_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:23 | / | / | / |
| 22 | R/W | 0x0 | LEAP. Leap Year. 0: not, 1: Leap year. This bit can not set by hardware. It should be set or clear by software. |
| 21:16 | R/W | x | YEAR. Year. Range from 0~63. |
| 15:12 | / | / | / |
| 11:8 | R/W | x | MONTH. Month. Range from 1~12. |
| 7:5 | / | / | / |
| 4:0 | R/W | x | DAY. Day. Range from 1~31. |

Note1: If the written value is not from 1 to 31 in Day Area, it turns into 31 automatically. Month Area and Year Area are similar to Day Area.

Note2: The number of days in different month may be different.

4.13.3.4. RTC HH-MM-SS Register (Default Value: 0x00000000)

| Offset: 0x14 | | | Register Name: RTC_HH_MM_SS_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | R/W | 0x0 | WK_NO. Week number. 000: Monday 001: Tuesday 010: Wednesday 011: Thursday 100: Friday 101: Saturday 110: Sunday 111: / |
| 28:21 | / | / | / |
| 20:16 | R/W | x | HOUR. |

| | | | |
|-------|-----|---|----------------------------|
| | | | Range from 0~23 |
| 15:14 | / | / | / |
| 13:8 | R/W | x | MINUTE. Range from 0~59 |
| 7:6 | / | / | / |
| 5:0 | R/W | x | SECOND. Range from 0~59 |

Note: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

4.13.3.5. Alarm 0 Counter Register (Default Value: 0x00000000)

| | | | |
|--------------|-----|-------------|--|
| Offset: 0x20 | | | Register Name: ALARM0_COUNTER_REG |
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | ALARM0_COUNTER. Alarm 0 Counter is based on Second. |

Note: If the second is set to 0, it will be 1 second in fact.

4.13.3.6. Alarm 0 Current Value Register (Default Value: 0x00000000)

| | | | |
|--------------|-----|-------------|--|
| Offset: 0x24 | | | Register Name: ALARM0_CUR_VLU_REG |
| Bit | R/W | Default/Hex | Description |
| 31:0 | RO | x | ALARM0_CUR_VLU. Check Alarm 0 Counter Current Values. |

Note: If the second is set to 0, it will be 1 second in fact.

4.13.3.7. Alarm 0 Enable Register (Default Value: 0x00000000)

| | | | |
|--------------|-----|-------------|---|
| Offset: 0x28 | | | Register Name: ALARM0_ENABLE_REG |
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | ALM_0_EN Alarm 0 Enable. If this bit is set to "1", the Alarm 0 Counter register's valid bits will down count to zero, and the alarm pending bit will be set to "1". 0: Disable 1: Enable |

4.13.3.8. Alarm 0 IRQ Enable Register (Default Value: 0x00000000)

| | | | |
|--------------|-----|-------------|---|
| Offset: 0x2C | | | Register Name: ALARM0_IRQ_EN_REG |
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | ALARM0_IRQ_EN. |

| | | | |
|--|--|--|--|
| | | | Alarm 0 IRQ Enable. 0: Disable 1: Enable |
|--|--|--|--|

4.13.3.9. Alarm 0 IRQ Status Register (Default Value: 0x00000000)

| Offset: 0x30 | | | Register Name: ALARM0_IRQ_STA_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | ALARM0_IRQ_PEND. Alarm 0 IRQ Pending bit. 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller. |

4.13.3.10. Alarm 1 Week HH-MM-SS Register (Default Value: 0x00000000)

| Offset: 0x40 | | | Register Name: ALARM0_WK_HH_MM-SS |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:21 | / | / | / |
| 20:16 | R/W | x | HOUR. Range from 0~23. |
| 15:14 | / | / | / |
| 13:8 | R/W | x | MINUTE. Range from 0~59. |
| 7:6 | / | / | / |
| 5:0 | R/W | x | SECOND. Range from 0~59. |

Note: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

4.13.3.11. Alarm 1 Enable Register (Default Value: 0x00000000)

| Offset: 0x44 | | | Register Name: ALARM1_EN_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:7 | / | / | / |
| 6 | R/W | 0x0 | WK6_ALM1_EN. Week 6 (Sunday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 6, the week 6 alarm irq pending bit will be set to "1". |
| 5 | R/W | 0x0 | WK5_ALM1_EN. Week 5 (Saturday) Alarm 1 Enable. 0: Disable 1: Enable |

| | | | |
|---|-----|-----|--|
| | | | If this bit is set to "1", only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 5, the week 5 alarm irq pending bit will be set to "1". |
| 4 | R/W | 0x0 | WK4_ALM1_EN. Week 4 (Friday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 4, the week 4 alarm irq pending bit will be set to "1". |
| 3 | R/W | 0x0 | WK3_ALM1_EN. Week 3 (Thursday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 3, the week 3 alarm irq pending bit will be set to "1". |
| 2 | R/W | 0x0 | WK2_ALM1_EN. Week 2 (Wednesday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 2, the week 2 alarm irq pending bit will be set to "1". |
| 1 | R/W | 0x0 | WK1_ALM1_EN. Week 1 (Tuesday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 1, the week 1 alarm irq pending bit will be set to "1". |
| 0 | R/W | 0x0 | WK0_ALM1_EN. Week 0 (Monday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 0, the week 0 alarm irq pending bit will be set to "1". |

4.13.3.12. Alarm 1 IRQ Enable Register (Default Value: 0x00000000)

| Offset: 0x48 | | | Register Name: ALARM1_IRQ_EN_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | ALARM1_IRQ_EN. Alarm 1 IRQ Enable. 0: Disable 1: Enable |

4.13.3.13. Alarm 1 IRQ Status Register (Default Value: 0x00000000)

| Offset: 0x4C | | | Register Name: ALARM1_IRQ_STA_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | ALARM1_WEEK_IRQ_PEND. Alarm 1 Week (0/1/2/3/4/5/6) IRQ Pending. 0: No effect 1: Pending, week counter value is reached If alarm 1 week irq enable is set to 1, the pending bit will be sent to the interrupt controller. |

4.13.3.14. Alarm Config Register (Default Value: 0x00000000)

| Offset: 0x50 | | | Register Name: ALARM_CONFIG_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | ALARM_WAKEUP. Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output |

4.13.3.15. LOSC Output Gating Register (Default Value: 0x00000000)

| Offset: 0x60 | | | Register Name: LOSC_OUT_GATING_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0x0 | LOSC_OUT_GATING. Configuration of LOSC output, and no LOSC output by default. 0: Enable LOSC output gating 1: Disable LOSC output gating |

4.13.3.16. LOSC Output Gating Register (Default Value: 0x00000000)

| Offset: 0x100+N*0x4(N=0~7) | | | Register Name: GP_DATA_REGn |
|----------------------------|-----|-------------|------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | GP_DATA. Data [31:0]. |

Note: General purpose register 0~7 value can be stored if the VDD_RTC is larger than 1.0v

4.13.3.17. VDD RTC Regulation Register (Default Value: 0x00000004)

| Offset: 0x190 | | | Register Name: VDD_RTC_REG |
|---------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:3 | / | / | / |

| | | | |
|-----|-----|-------|--|
| 2:0 | R/W | 0x100 | <p>VDD_RTC_REGU.</p> <p>These bits are useful for regulating the RTC_VIO from 0.7v to 1.4v, and the regulation step is 0.1v.</p> <p>000: 0.7v 001: 0.8v 010: 0.9v 011: 1.0v 100: 1.1v 101: 1.2v 110: 1.3v 111: 1.4v</p> |
|-----|-----|-------|--|

4.13.3.18. IC Characteristic Register (Default Value: 0x00000000)

| Offset: 0x1F0 | | | Register Name: IC_CHARA_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:16 | R/W | 0x0 | <p>IC_CHARA.</p> <p>Key Field.</p> <p>Should be written at value 0x16AA. Writing any other value in this field aborts the write operation.</p> |
| 15:0 | R/W | 0x0 | <p>ID_DATA.</p> <p>Return 0x16AA only if the KEY_FIELD is set as 0x16AA when read those bits, otherwise return 0x0.</p> |

4.14. Audio Codec

4.14.1. Overview

The embedded Audio Codec is a high-quality stereo audio codec designed for embed device. It provides a stereo DAC for playback, and a stereo ADC for recording.

The feature of Audio Codec:

- Two audio digital-to-analog(DAC) channels
- Two audio analog-to-digital(ADC) channels
 - 92dB SNR@A-weight
 - Supports ADC Sample Rates from 8KHz to 48KHz
- Support analog/ digital volume control
- Two low-noise analog microphone bias outputs
- Analog low-power loop from microphone to headphone outputs
- Support Dynamic Range Controller adjusting the DAC playback output(DRC)
- Four audio inputs:
 - Three differential microphone inputs
 - Stereo Linein input
- Two audio outputs:
 - Stereo Headphone output
 - Differential Lineout output
- Support Automatic Gain Control(AGC) and Dynamic Range Control(DRC) adjusting the ADC recording input
- Interrupt and DMA Support

4.14.2. Power and Signal Description

4.14.2.1. Analog I/O Pins

| Signal Name | Type | Description |
|-------------|------|----------------------------------|
| MIC1P | I | First microphone positive input |
| MIC1N | I | First microphone negative input |
| MIC2P | I | Second microphone positive input |
| MIC2N | I | Second microphone negative input |
| MIC3P | I | Third microphone positive input |
| MIC3N | I | Third microphone negative input |
| HPOUTL | O | Headphone left output |
| HPOUTR | O | Headphone right output |
| HPCOM | O | HPCOM output |
| HPCOMFB | I | HPCOM feedback input |
| LINEINL | I | Linein left input |
| LINEINR | I | Linein right input |
| LINEOUTP | O | Lineout positive output |
| LINEOUTN | O | Lineout negative output |

4.14.2.2. Filter/Reference

| | | |
|---------|---|--|
| MBIAS | O | Bias voltage output for main microphone |
| HBIAS | O | Bias voltage output for headphone microphone |
| VRA2 | O | internal reference voltage |
| HPVCCBP | O | HPVCC bypass |

4.14.2.3. Power/Ground

| | | |
|---------|---|---------------------------|
| AVCC | P | Analog power |
| HPVCCIN | P | Headphone amplifier power |
| AGND | G | Analog ground |

4.14.3. Data Path Diagram

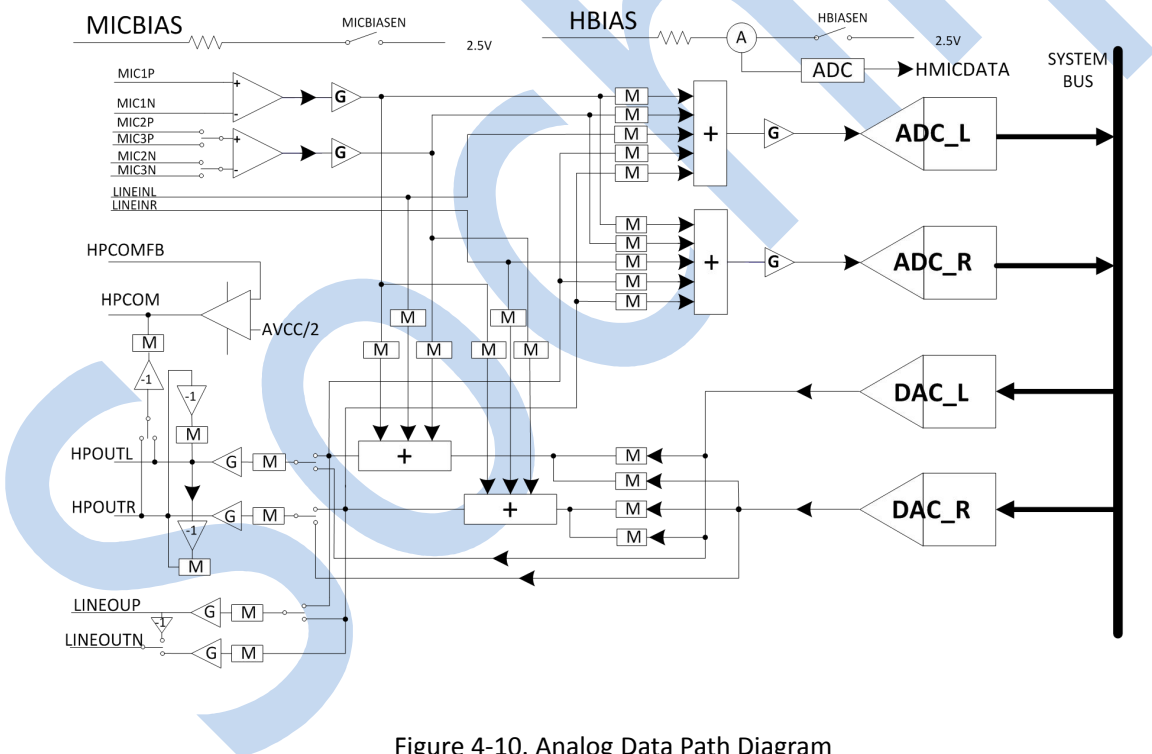


Figure 4-10. Analog Data Path Diagram

4.14.4. Audio Codec Register List

| Module Name | Base Address |
|-------------|--------------|
| AC | 0x01C22C00 |

| Register Name | Offset | Description |
|---------------|--------|-----------------------------------|
| AC_DAC_DPC | 0x000 | DAC Digital Part Control Register |

| | | |
|--------------------|-------|---|
| AC_DAC_FIFOC | 0x004 | DAC FIFO Control Register |
| AC_DAC_FIFOS | 0x008 | DAC FIFO Status Register |
| AC_ADC_FIFOC | 0x010 | ADC FIFO Control Register |
| AC_ADC_FIFOS | 0x014 | ADC FIFO Status Register |
| AC_ADC_RXDATA | 0x018 | ADC RX Data Register |
| AC_DAC_TXDATA | 0x020 | DAC TX Data Register |
| AC_DAC_CNT | 0x040 | DAC TX FIFO Counter Register |
| AC_ADC_CNT | 0x044 | ADC RX FIFO Counter Register |
| AC_DAC_DG | 0x048 | DAC Debug Register |
| AC_ADC_DG | 0x04C | ADC Debug Register |
| AC_DAC_DAP_CTR | 0x060 | DAC DAP Control Register |
| AC_ADC_DAP_CTR | 0x070 | ADC DAP Control Register |
| AC_ADC_DAP_LCTR | 0x074 | ADC DAP Left Control Register |
| AC_ADC_DAP_RCTR | 0x078 | ADC DAP Right Control Register |
| AC_ADC_DAP_PARA | 0x07C | ADC DAP Parameter Register |
| AC_ADC_DAP_LAC | 0x080 | ADC DAP Left Average Coef Register |
| AC_ADC_DAP_LDAT | 0x084 | ADC DAP Left Decay and Attack Time Register |
| AC_ADC_DAP_RAC | 0x088 | ADC DAP Right Average Coef Register |
| AC_ADC_DAP_RDAT | 0x08C | ADC DAP Right Decay and Attack Time Register |
| ADC_DAP_HPFC | 0x090 | ADC DAP HPF Coef Register |
| ADC_DAP_LINAC | 0x094 | ADC DAP Left Input Signal Low Average Coef Register |
| ADC_DAP_RINAC | 0x098 | ADC DAP Right Input Signal Low Average Coef Register |
| ADC_DAP_ORT | 0x09C | ADC DAP Optimum Register |
| AC_DAC_DRC_HHPFC | 0x100 | DAC DRC High HPF Coef Register |
| AC_DAC_DRC_LHPFC | 0x104 | DAC DRC Low HPF Coef Register |
| AC_DAC_DRC_CTRL | 0x108 | DAC DRC Control Register |
| AC_DAC_DRC_LPFHAT | 0x10C | DAC DRC Left Peak Filter High Attack Time Coef Register |
| AC_DAC_DRC_LPFLAT | 0x110 | DAC DRC Left Peak Filter Low Attack Time Coef Register |
| AC_DAC_DRC_RPFHAT | 0x114 | DAC DRC Right Peak Filter High Attack Time Coef Register |
| AC_DAC_DRC_RPFLAT | 0x118 | DAC DRC Peak Filter Low Attack Time Coef Register |
| AC_DAC_DRC_LPFHRT | 0x11C | DAC DRC Left Peak Filter High Release Time Coef Register |
| AC_DAC_DRC_LPFLRT | 0x120 | DAC DRC Left Peak Filter Low Release Time Coef Register |
| AC_DAC_DRC_RPFHRT | 0x124 | DAC DRC Right Peak filter High Release Time Coef Register |
| AC_DAC_DRC_RPFLRT | 0x128 | DAC DRC Right Peak filter Low Release Time Coef Register |
| AC_DAC_DRC_LRMSHAT | 0x12C | DAC DRC Left RMS Filter High Coef Register |
| AC_DAC_DRC_LRMSLAT | 0x130 | DAC DRC Left RMS Filter Low Coef Register |
| AC_DAC_DRC_RRMSHAT | 0x134 | DAC DRC Right RMS Filter High Coef Register |
| AC_DAC_DRC_RRMSLAT | 0x138 | DAC DRC Right RMS Filter Low Coef Register |
| AC_DAC_DRC_HCT | 0x13C | DAC DRC Compressor Theshold High Setting Register |
| AC_DAC_DRC_LCT | 0x140 | DAC DRC Compressor Slope High Setting Register |
| AC_DAC_DRC_HKC | 0x144 | DAC DRC Compressor Slope High Setting Register |
| AC_DAC_DRC_LKC | 0x148 | DAC DRC Compressor Slope Low Setting Register |
| AC_DAC_DRC_HOPC | 0x14C | DAC DRC Compressor High Output at Compressor Threshold Register |
| AC_DAC_DRC_LOPC | 0x150 | DAC DRC Compressor Low Output at Compressor Threshold Register |
| AC_DAC_DRC_HLT | 0x154 | DAC DRC Limiter Theshold High Setting Register |
| AC_DAC_DRC_LLT | 0x158 | DAC DRC Limiter Theshold Low Setting Register |

| | | |
|---------------------|--------|---|
| AC_DAC_DRC_HKI | 0x15C | DAC DRC Limiter Slope High Setting Register |
| AC_DAC_DRC_LKI | 0x160 | DAC DRC Limiter Slope Low Setting Register |
| AC_DAC_DRC_HOPL | 0x164 | DAC DRC Limiter High Output at Limiter Threshold |
| AC_DAC_DRC_LOPL | 0x168 | DAC DRC Limiter Low Output at Limiter Threshold |
| AC_DAC_DRC_HET | 0x16C | DAC DRC Expander Theshold High Setting Register |
| AC_DAC_DRC_LET | 0x170 | DAC DRC Expander Theshold Low Setting Register |
| AC_DAC_DRC_HKE | 0x174 | DAC DRC Expander Slope High Setting Register |
| AC_DAC_DRC_LKE | 0x178 | DAC DRC Expander Slope Low Setting Register |
| AC_DAC_DRC_HOPE | 0x17C | DAC DRC Expander High Output at Expander Threshold |
| AC_DAC_DRC_LOPE | 0x180 | DAC DRC Expander Low Output at Expander Threshold |
| AC_DAC_DRC_HKN | 0x184 | DAC DRC Linear Slope High Setting Register |
| AC_DAC_DRC_LKN | 0x188 | DAC DRC Linear Slope Low Setting Register |
| AC_DAC_DRC_SFHAT | 0x18C | DAC DRC Smooth filter Gain High Attack Time Coef Register |
| AC_DAC_DRC_SFLAT | 0x190 | DAC DRC Smooth filter Gain Low Attack Time Coef Register |
| AC_DAC_DRC_SFHRT | 0x194 | DAC DRC Smooth filter Gain High Release Time Coef Register |
| AC_DAC_DRC_SFLRT | 0x198 | DAC DRC Smooth filter Gain Low Release Time Coef Register |
| AC_DAC_DRC_MXGHS | 0x19C | DAC DRC MAX Gain High Setting Register |
| AC_DAC_DRC_MXGLS | 0x1A0 | DAC DRC MAX Gain Low Setting Register |
| AC_DAC_DRC_MNGHS | 0x1A4 | DAC DRC MIN Gain High Setting Register |
| AC_DAC_DRC_MNGLS | 0x1A8 | DAC DRC MIN Gain Low Setting Register |
| AC_DAC_DRC_EPSHC | 0x1AC | DAC DRC Expander Smooth Time High Coef Register |
| AC_DAC_DRC_EPSLC | 0x1B0 | DAC DRC Expander Smooth Time Low Coef Register |
| AC_DAC_DRC_HPFHGAIN | 0x 1B8 | DAC DRC HPF Gain High |
| AC_DAC_DRC_HPFLGAIN | 0x1BC | DAC DRC HPF Gain Low |
| AC_ADC_DRC_HHPFC | 0x200 | ADC DRC High HPF Coef Register |
| AC_ADC_DRC_LHPFC | 0x204 | ADC DRC Low HPF Coef Register |
| AC_ADC_DRC_CTRL | 0x208 | ADC DRC Control Register |
| AC_ADC_DRC_LPFHAT | 0x20C | ADC DRC Left Peak Filter High Attack Time Coef Register |
| AC_ADC_DRC_LPFLAT | 0x210 | ADC DRC Left Peak Filter Low Attack Time Coef Register |
| AC_ADC_DRC_RPFHAT | 0x214 | ADC DRC Right Peak Filter High Attack Time Coef Register |
| AC_ADC_DRC_RPFLAT | 0x218 | ADC DRC Peak Filter Low Attack Time Coef Register |
| AC_ADC_DRC_LPFHRT | 0x21C | ADC DRC Left Peak Filter High Release Time Coef Register |
| AC_ADC_DRC_LPFLRT | 0x220 | ADC DRC Left Peak Filter Low Release Time Coef Register |
| AC_ADC_DRC_RPFHRT | 0x224 | ADC DRC Right Peak filter High Release Time Coef Register |
| AC_ADC_DRC_RPFLRT | 0x228 | ADC DRC Right Peak filter Low Release Time Coef Register |
| AC_ADC_DRC_LRMSHAT | 0x22C | ADC DRC Left RMS Filter High Coef Register |
| AC_ADC_DRC_LRMSLAT | 0x230 | ADC DRC Left RMS Filter Low Coef Register |
| AC_ADC_DRC_RRMSHAT | 0x234 | ADC DRC Right RMS Filter High Coef Register |
| AC_ADC_DRC_RRMSLAT | 0x238 | ADC DRC Right RMS Filter Low Coef Register |
| AC_ADC_DRC_HCT | 0x23C | ADC DRC Compressor Theshold High Setting Register |
| AC_ADC_DRC_LCT | 0x240 | ADC DRC Compressor Slope High Setting Register |
| AC_ADC_DRC_HKC | 0x244 | ADC DRC Compressor Slope High Setting Register |
| AC_ADC_DRC_LKC | 0x248 | ADC DRC Compressor Slope Low Setting Register |
| AC_ADC_DRC_HOPC | 0x24C | ADC DRC Compressor High Output at Compressor Threshold Register |

| | | |
|------------------------|--------|--|
| AC_ADC_DRC_LOPC | 0x250 | ADC DRC Compressor Low Output at Compressor Threshold Register |
| AC_ADC_DRC_HLT | 0x254 | ADC DRC Limiter Theshold High Setting Register |
| AC_ADC_DRC_LLT | 0x258 | ADC DRC Limiter Theshold Low Setting Register |
| AC_ADC_DRC_HKI | 0x25C | ADC DRC Limiter Slope High Setting Register |
| AC_ADC_DRC_LKI | 0x260 | ADC DRC Limiter Slope Low Setting Register |
| AC_ADC_DRC_HOPL | 0x264 | ADC DRC Limiter High Output at Limiter Threshold |
| AC_ADC_DRC_LOPL | 0x268 | ADC DRC Limiter Low Output at Limiter Threshold |
| AC_ADC_DRC_HET | 0x26C | ADC DRC Expander Theshold High Setting Register |
| AC_ADC_DRC_LET | 0x270 | ADC DRC Expander Theshold Low Setting Register |
| AC_ADC_DRC_HKE | 0x274 | ADC DRC Expander Slope High Setting Register |
| AC_ADC_DRC_LKE | 0x278 | ADC DRC Expander Slope Low Setting Register |
| AC_ADC_DRC_HOPE | 0x27C | ADC DRC Expander High Output at Expander Threshold |
| AC_ADC_DRC_LOPE | 0x280 | ADC DRC Expander Low Output at Expander Threshold |
| AC_ADC_DRC_HKN | 0x284 | ADC DRC Linear Slope High Setting Register |
| AC_ADC_DRC_LKN | 0x288 | ADC DRC Linear Slope Low Setting Register |
| AC_ADC_DRC_SFHAT | 0x28C | ADC DRC Smooth filter Gain High Attack Time Coef Register |
| AC_ADC_DRC_SFLAT | 0x290 | ADC DRC Smooth filter Gain Low Attack Time Coef Register |
| AC_ADC_DRC_SFHRT | 0x294 | ADC DRC Smooth filter Gain High Release Time Coef Register |
| AC_ADC_DRC_SFLRT | 0x298 | ADC DRC Smooth filter Gain Low Release Time Coef Register |
| AC_ADC_DRC_MXGHS | 0x29C | ADC DRC MAX Gain High Setting Register |
| AC_ADC_DRC_MXGLS | 0x2A0 | ADC DRC MAX Gain Low Setting Register |
| AC_ADC_DRC_MNGLS | 0x2A4 | ADC DRC MIN Gain High Setting Register |
| AC_ADC_DRC_MXGLS | 0x2A8 | ADC DRC MIN Gain Low Setting Register |
| AC_ADC_DRC_EPSHC | 0x2AC | ADC DRC Expander Smooth Time High Coef Register |
| AC_ADC_DRC_EPSLC | 0x2B0 | ADC DRC Expander Smooth Time Low Coef Register |
| AC_ADC_DRC_HPFGAIN | 0x 2B8 | ADC DRC HPF Gain High |
| AC_ADC_DRC_HPFLGAIN | 0x2BC | ADC DRC HPF Gain Low |
| AC_PR_CFG | 0x400 | AC Parameter Configuration Register |
| Analog Domain Register | | |
| AC_PAG_HPVC | 0x00 | PA clock gating and Headphone Volume Control |
| AC_LOMIXSC | 0x01 | Left Output Mixer Source Select Control Register |
| AC_ROMIXSC | 0x02 | Right Output Mixer Source Select Control Register |
| DAC_PA_SRC | 0x03 | DAC Analog Enable and PA Source Control Register |
| MIC_GCTR | 0x06 | MIC1 And MIC2 Gain Control Register |
| HP_CTRL | 0x07 | HP Control |
| MIC2_LINE_CTRL | 0x0A | MIC2 Boost LINE-OUT Enable and Source select |
| BIAS_MIC_CTRL | 0x0B | BIAS 、 MIC2 Source and MIC1 boost |
| LADC_MIX_MUTE | 0x0C | Left ADC Mixer Mute Control |
| RADC_MIX_MUTE | 0x0D | Right ADC Mixer Mute Control |
| PA_ANTI_POP_CTRL | 0x0E | PA Anti-pop time Control |
| AC_ADC_CTRL | 0x0F | ADC Analog Control Register |
| OPADC_CTRL | 0x10 | OPDRV/OPCOM 、 OPADC Control |
| OPMIC_CTRL | 0x11 | OPMIC、 OPVR and OPADC Control |
| ZERO_CROSS_CTRL | 0x12 | Zero Cross Control |

| | | |
|------------------|------|--|
| ADC_FUN_CTRL | 0x13 | ADC Function Control |
| CALIBRATION_CTRL | 0x14 | Bias & DA16 Calibration Control Register |
| DA16CALI_DATA | 0x15 | DA16 Calibration Data |
| BIAS16CALI_DATA | 0x17 | Bias Calibration Data |
| BIAS16CALI_SET | 0x18 | Bias Register Setting Data |

4.14.5. Audio Codec Register Description

4.14.5.1. 0x000 DAC Digital Part Control Register(Default Value: 0x00000000)

| Offset: 0x000 | | | Register Name: AC_DAC_DPC |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | EN_DAC DAC Digital Part Enable 0 : Disable 1 : Enable |
| 30:29 | / | / | / |
| 28:25 | R/W | 0x0 | MODQU Internal DAC Quantization Levels Levels= $[7*(21+MODQU[3:0])]/128$ Default levels= $7*21/128=1.15$ |
| 24:19 | / | / | / |
| 18 | R/W | 0x0 | HPF_EN High Pass Filter Enable 0: Disable 1: Enable |
| 17:12 | R/W | 0x0 | DVOL Digital volume control: DVC, ATT=DVC[5:0]*(-1.16Db) 64 steps, -1.16dB/step |
| 11:0 | / | / | / |

4.14.5.2. 0x004 DAC FIFO Control Register(Default Value: 0x00000F00)

| Offset: 0x004 | | | Register Name: AC_DAC_FIFOC |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:29 | R/W | 0x0 | DAC_FS Sample Rate of DAC 000: 48KHz 010: 24KHz 100: 12KHz 110: 192KHz 001: 32KHz 011: 16KHz 101: 8KHz 111: 96KHz 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit |
| 28 | R/W | 0x0 | FIR_VER FIR Version 0: 64-Tap FIR; 1: 32-Tap FIR |
| 27 | / | / | / |

| | | | |
|-------|-----|-----|---|
| 26 | R/W | 0x0 | SEND_LASAT Audio sample select when TX FIFO underrun 0: Sending zero 1: Sending last audio sample |
| 25:24 | R/W | 0x0 | FIFO_MODE For 24-bits transmitted audio sample: 00/10: FIFO_I[23:0] = {TXDATA[31:8]} 01/11: Reserved For 16-bits transmitted audio sample: 00/10: FIFO_I[23:0] = {TXDATA[31:16], 8'b0} 01/11: FIFO_I[23:0] = {TXDATA[15:0], 8'b0} |
| 23 | / | / | / |
| 22:21 | R/W | 0x0 | DAC_DRQ_CLR_CNT When TX FIFO available room is less than or equal N, DRQ request will be de-asserted. N is defined here: 00: IRQ/DRQ De-Asserted When WLEVEL > TXTL 01: 4 10: 8 11: 16 |
| 20:15 | / | / | / |
| 14:8 | R/W | 0xF | TX_TRIG_LEVEL TX FIFO Empty Trigger Level (TXTL[12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ is generated when WLEVEL ≤ TXTL Notes: 1. WLEVEL represents the number of valid samples in the TX FIFO 2. Only TXTL[6:0] valid when TXMODE = 0 |
| 7 | R/W | 0x0 | ADDA_LOOP_EN ADDA Loop Enable 0: Disable 1: Enable |
| 6 | R/W | 0x0 | DAC_MONO_EN DAC Mono Enable 0: Stereo, 64 Levels FIFO 1: Mono, 128 Levels FIFO When Enabled, L & R Channel Send Same Data |
| 5 | R/W | 0x0 | TX_SAMPLE_BITS Transmitting Audio Sample Resolution 0: 16 bits 1: 24 bits |
| 4 | R/W | 0x0 | DAC_DRQ_EN DAC FIFO Empty DRQ Enable 0: Disable 1: Enable |
| 3 | R/W | 0x0 | DAC_IRQ_EN DAC FIFO Empty IRQ Enable 0: Disable 1: Enable |
| 2 | R/W | 0x0 | FIFO_UNDERRUN_IRQ_EN DAC FIFO Underrun IRQ Enable 0: Disable 1: Enable |
| 1 | R/W | 0x0 | FIFO_OVERRUN_IRQ_EN DAC FIFO Overrun IRQ Enable |

| | | | |
|---|-----|-----|---|
| | | | 0: Disable 1: Enable |
| 0 | R/W | 0x0 | FIFO_FLUSH DAC FIFO Flush Write '1' To Flush TX FIFO, Self Clear to '0' |

4.14.5.3. 0x008 DAC FIFO Status Register(Default Value: 0x00800088)

| Offset: 0x008 | | | Register Name: AC_DAC_FIFOS |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23 | R | 0x1 | TX_EMPTY TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word) |
| 22:8 | R | 0x80 | TXE_CNT TX FIFO Empty Space Word Counter |
| 7:4 | / | / | / |
| 3 | R/W | 0x1 | TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatic clear if interrupt condition fails |
| 2 | R/W | 0x0 | TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Underrun Pending Interrupt Write '1' to clear this interrupt |
| 1 | R/W | 0x0 | TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt |
| 0 | / | / | / |

4.14.5.4. 0x010 ADC FIFO Control Register(Default Value: 0x00000F00)

| Offset: 0x010 | | | Register Name: AC_ADC_FIFOC |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | R/W | 0x0 | ADFS Sample Rate of ADC 000: 48KHz 010: 24KHz 100: 12KHz 110: Reserved 001: 32KHz 011: 16KHz 101: 8KHz 111: Reserved 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit |
| 28 | R/W | 0x0 | EN_AD |

| | | | |
|-------|-----|-----|--|
| | | | ADC Digital Part Enable 0: Disable 1: Enable |
| 27:25 | / | / | / |
| 24 | R/W | 0x0 | RX_FIFO_MODE RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 24-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:0], 8'h0} Mode 1: Reserved For 16-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:8], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[23]}, FIFO_O[23:8]} |
| 23:19 | / | / | / |
| 18:17 | R/W | 0x0 | ADCFDT ADC FIFO Delay Time for Writing Data after EN_AD 00:5ms 01:10ms 10:20ms 11:30ms |
| 16 | R/W | 0x0 | ADCFDEN ADC FIFO Delay Function for Writing Data after EN_AD 0: Disable 1: Enable |
| 15:13 | / | / | / |
| 12:8 | R/W | 0xF | RX_FIFO_TRG_LEVEL RX FIFO Trigger Level (RXTL[4:0]) Interrupt and DMA request trigger level for RX FIFO normal condition IRQ/DRQ Generated when WLEVEL > RXTL[4:0] Notes: WLEVEL represents the number of valid samples in the RX FIFO |
| 7 | R/W | 0x0 | ADC_MONO_EN ADC Mono Enable 0: Stereo, 16 levels FIFO 1: mono, 32 levels FIFO When set to '1', Only left channel samples are recorded |
| 6 | R/W | 0x0 | RX_SAMPLE_BITS Receiving Audio Sample Resolution 0: 16 bits 1: 24 bits |
| 5 | / | / | / |
| 4 | R/W | 0x0 | ADC_DRQ_EN ADC FIFO Data Available DRQ Enable 0: Disable 1: Enable |
| 3 | R/W | 0x0 | ADC_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable |
| 2 | / | / | / |
| 1 | R/W | 0x0 | ADC_OVERRUN_IRQ_EN ADC FIFO Over Run IRQ Enable 0: Disable |

| | | | |
|---|-----|-----|---|
| | | | 1: Enable |
| 0 | R/W | 0x0 | ADC_FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self clear to '0' |

4.14.5.5. 0x014 ADC FIFO Status Register(Default Value: 0x00000000)

| Offset: 0x014 | | | Register Name: AC_ADC_FIFOS |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23 | R | 0x0 | RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word) |
| 22:14 | / | / | / |
| 13:8 | R | 0x0 | RXA_CNT RX FIFO Available Sample Word Counter |
| 7:4 | / | / | / |
| 3 | R/W | 0x0 | RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails |
| 2 | / | / | / |
| 1 | R/W | 0x0 | RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt |
| 0 | / | / | / |

4.14.5.6. 0x018 ADC RX DATA Register(Default Value: 0x00000000)

| Offset: 0x018 | | | Register Name: AC_ADC_RXDATA |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0x0 | RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample. |

4.14.5.7. 0x020 DAC TX DATA Register(Default Value: 0x00000000)

| Offset: 0x020 | | | Register Name: AC_DAC_TXDATA |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | W | 0x0 | TX_DATA Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample |

4.14.5.8. 0x040 DAC TX Counter Register(Default Value: 0x00000000)

| Offset: 0x040 | | | Register Name: AC_DAC_CNT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value Notes: It is used for Audio/ Video Synchronization |

4.14.5.9. 0x044 ADC RX Counter Register(Default Value: 0x00000000)

| Offset: 0x044 | | | Register Name: AC_ADC_CNT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value Notes: It is used for Audio/ Video Synchronization |

4.14.5.10. 0x048 DAC Debug Register(Default Value: 0x00000000)

| Offset: 0x048 | | | Register Name: AC_DAC_DG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:12 | / | / | / |
| 11 | R/W | 0x0 | DAC_MODU_SELECT DAC Modulator Debug 0: DAC Modulator Normal Mode 1: DAC Modulator Debug Mode |
| 10:9 | R/W | 0x0 | DAC_PATTERN_SELECT. DAC Pattern Select 00: Normal (Audio Sample from TX FIFO) 01: -6 dB Sin wave 10: -60 dB Sin wave 11: silent wave |
| 8 | R/W | 0x0 | CODEC_CLK_SELECT CODEC Clock Source Select 0: CODEC Clock from PLL 1: CODEC Clock from OSC (For Debug) |
| 7 | / | / | / |
| 6 | R/W | 0x0 | DA_SWP DAC output channel swap enable 0:Disable 1:Enable |

| | | | |
|-----|---|---|---|
| 5:0 | / | / | / |
|-----|---|---|---|

4.14.5.11. 0x04C ADC Debug Register(Default Value: 0x00000000)

| Offset: 0x4C | | | Register Name: AC_ADC_DG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:25 | / | / | / |
| 24 | R/W | 0x0 | AD_SWP ADC Output Channel Swap Enable (for digital filter) 0: Disable 1: Enable |
| 23:0 | / | / | / |

4.14.5.12. 0x050 HMIC Control Register(Default Value: 0x00000000)

| Offset: 0x50 | | | Register Name: HMIC_CTRL |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | R/W | 0x0 | HMIC_M Debounce when key down or key up |
| 27:24 | R/W | 0x0 | HMIC_N Debounce when earphone plug in or pull out |
| 23 | R/W | 0x0 | HMIC_DATA_IRQ_MODE Hmic Data Irq Mode Select 0: Hmic data irq once after key down 1: Hmic data irq from key down, until key up |
| 22:21 | R/W | 0x0 | HMIC_TH1_HYSTERESIS Hmic Hysteresis Threshold1 00: no Hysteresis 01: Pull Out when Data <= (Hmic_th2-1) 10: Pull Out when Data <= (Hmic_th2-2) 11: Pull Out when Data <= (Hmic_th2-3) |
| 20 | R/W | 0x0 | HMIC_PULLOUT_IRQ Hmic Earphone Pull out Irq Enable 00: disable, 11: enable |
| 19 | R/W | 0x0 | HMIC_PLUGIN_IRQ Hmic Earphone Plug in Irq Enable 00: disable 11: enable |
| 18 | R/W | 0x0 | HMIC_KEYUP_IRQ Hmic Key Up Irq Enable 00: disable 11: enable |
| 17 | R/W | 0x0 | HMIC_KEYDOWN_IRQ Hmic Key Down Irq Enable 00: disable 11: enable |
| 16 | R/W | 0x0 | HMIC_DATA_IRQ_EN Hmic Data Irq Enable 00: disable 11: enable |
| 15:14 | R/W | 0x0 | HMIC_SAMPLE_SELECT Down Sample Setting Select 00: Down by 1, 128Hz 01: Down by 2, 64Hz 10: Down by 4, 32Hz |

| | | | |
|------|-----|-----|--|
| | | | 11: Down by 8, 16Hz |
| 13 | R/W | 0x0 | HMIC_TH2_HYSTERESIS Hmic Hysteresis Threshold2 0: no Hysteresis 1: Key Up when Data <= (Hmic_th2-1) |
| 12:8 | R/W | 0x0 | HMIC_TH2 Hmic_th2 for detecting Key down or Key up. |
| 7:6 | R/W | 0x0 | HMIC_SF Hmic Smooth Filter setting 00: by pass 01: (x1+x2)/2 10: (x1+x2+x3+x4)/4 11: (x1+x2+x3+x4+ x5+x6+x7+x8)/8 |
| 5 | R/W | 0x0 | KEYUP_CLEAR Key Up Irq Pending bit auto clear when Key Down Irq 0: don't clear 1: auto clear |
| 4:0 | R/W | 0x0 | HMIC_TH1 Hmic_th1[4:0], detecting eraphone plug in or pull out. |

4.14.5.13. 0x054 HMIC Data Register(Default Value: 0x00000000)

| Offset: 0x54 | | | Register Name: HMIC_DATA |
|--------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 31:21 | / | / | / |
| 20 | R/W | 0x0 | HMIC_PULLOUT_PENDING Hmic Earphone Pull out Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Pull out Irq Pending Interrupt |
| 19 | R/W | 0x0 | HMIC_PLUGIN_PENDING Hmic Earphone Plug in Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Plug in Irq Pending Interrupt |
| 18 | R/W | 0x0 | HMIC_KEYUP_PENDING Hmic Key Up Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Key up Irq Pending Interrupt |
| 17 | R/W | 0x0 | HMIC_KEYDOWN_PENDING Hmic Key Down Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Key down Irq Pending Interrupt |
| 16 | R/W | 0x0 | HMIC_DATA_PENDING Hmic Data Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Data Irq Pending Interrupt |
| 15:5 | / | / | / |
| 4:0 | R | 0x0 | HMIC_DATA HMIC ADC Data |

4.14.5.14. 0x060 DAC DAP Control Register(Default Value: 0x00000000)

| Offset: 0x060 | | | Register Name: AC_DAC_DAP_CTR |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | DDAP_EN DAP for dac Enable 0 : bypass 1 : enable |
| 30:16 | / | / | / |
| 15 | R/W | 0x0 | DDAP_DRC_EN DRC enable control 0:disable 1:enable |
| 14 | R/W | 0x0 | DDAP_HPF_EN HPF enable control 0:disable 1:enable |
| 13:0 | / | / | / |

4.14.5.15. 0x070 ADC DAP Control Register(Default Value: 0x00000000)

| Offset: 0x070 | | | Register Name: AC_ADC_DAP_CTR |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | ADAP_EN DAP for ADC enable 0 : bypass 1 : enable |
| 30 | R/W | 0x0 | ADAP_START. DAP for ADC start up 0 : disable 1 : start up |
| 29:27 | / | / | / |
| 26 | R/W | 0x0 | ENADC_DRC DRC for ADC enable 0 : bypass 1 : enable |
| 25 | R/W | 0x0 | ADC_DRC_EN ADC DRC function enable 0 : disable 1 : enable |
| 24 | R/W | 0x0 | ADC_DRC_HPF_EN ADC DRC HPF function enable 0 : disable 1 : enable |
| 23:22 | | | |
| 21 | R | 0x0 | ADAP_LSATU_FLAG. Left channel AGC saturation flag 0 : no saturation 1 : saturation |
| 20 | R | 0x0 | ADAP_LNOI_FLAG. Left channel AGC noise-threshold flag |
| 19:12 | R | 0x0 | ADAP_LCHAN_GAIN |

| | | | |
|-------|---|-----|---|
| | | | Left channel Gain applied by AGC (7.1format 2s component(-20dB – 40dB), 0.5dB/ step) 0x50 : 40dB 0x4F : 39.5dB ----- 0x00 : 00dB 0xFF : -0.5dB |
| 11:10 | / | / | / |
| 9 | R | 0x0 | ADAP_RSATU_FLAG. Right AGC saturation flag 0 : no saturation 1: saturation |
| 8 | R | 0x0 | ADAP_RNOI_FLAG. Right channel AGC noise-threshold flag |
| 7:0 | R | 0x0 | ADAP_LCHAN_GAIN. Right Channel Gain applied by AGC (7.1format 2s component)(0.5dB step) 0x50 : 40dB 0x4F : 39.5dB ----- 0x00 : 00dB 0xFF : -0.5dB |

4.14.5.16. 0x074 ADC DAP Left Control Register(Default Value: 0x001F1800)

| Offset: 0x074 | | | Register Name: AC_ADC_DAP_LCTR |
|---------------|-----|---------------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:16 | R/W | 0x1F (-86dB) | ADAP_LNOI_SET. Left channel noise threshold setting 0x00 : -24dB 0x01 : -26dB 0x02 : -28dB ----- 0x1D: -82dB 0x1E: -84dB 0x1F: -86dB |
| 15 | / | / | / |
| 14 | R/W | 0x1 | AAGC_LCHAN_EN. Left AGC function enable 0:disable 1: enable |
| 13 | R/W | 0x1 | ADAP_LHPF_EN. Left HPF enable 0: disable 1: enable |
| 12 | R/W | 0x1 | ADAP_LNOI_DET. Left Noise detect enable 0: disable 1: enable |
| 11:10 | / | / | / |
| 9:8 | R/W | 0x0 | ADAP_LCHAN_HYS. Left Hysteresis setting |

| | | | |
|-----|-----|-----|--|
| | | | 00 : 1dB 01 : 2dB 10 : 4dB 11 : disable |
| 7:4 | R/W | 0x0 | ADAP_LNOI_DEB. Left Noise debounce time 0000:0/fs 0001:4/fs 0010:8/fs ----- 1111 :16*4096/fs $T=2(N+1)/fs$,except N=0 |
| 3:0 | R/W | 0x0 | ADAP_LSIG_DEB. Left Signal debounce time 0000:0/fs 0001:4/fs 0010:8/fs ----- 1111 :16*4096/fs $T=2(N+1)/fs$,except N=0 |

4.14.5.17. 0x078 ADC DAP Right Control Register(Default Value: 0x001F7000)

| Offset: 0x078 | | | Register Name: AC_ADC_DAP_RCTR |
|---------------|-----|-----------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:21 | / | / | / |
| 20:16 | R/W | 0x1F (-86dB) | ADAP_RNOI_SET. Right channel noise threshold setting 0x00 : -24dB 0x01 : -26dB 0x02 : -28dB ----- 0x1D: -82dB 0x1E: -84dB 0x1F: -86dB |
| 15 | / | / | / |
| 14 | R/W | 0x1 | AAGC_RCHAN_EN. Right AGC enable 0:disable 1:enable |
| 13 | R/W | 0x1 | ADAP_RHPF_EN. Right HPF enable 0: disable 1: enable |
| 12 | R/W | 0x1 | ADAP_RNOI_DET. Right Noise detect enable 0: disable 1:enable |
| 11:10 | / | / | / |
| 9:8 | R/W | 0x0 | ADAP_RCHAN_HYS. Right Hysteresis setting 00 : 1dB 01 : 2dB |

| | | | |
|-----|-----|-----|---|
| | | | 10 : 4dB 11 : disable; |
| 7:4 | R/W | 0x0 | ADAP_RNOI_DEB. Right Noise debounce time 0000:0/fs 0001:4/fs 0010:8/fs ----- 1111: 16*4096/fs T=2(N+1)/fs ,except N=0 |
| 3:0 | R/W | 0x0 | ADAP_RSIG_DEB. Right Signal debounce time 0000:0/fs 0001:4/fs 0010:8/fs ----- 1111: 16*4096/fs T=2(N+1)/fs ,except N=0 |

4.14.5.18. 0x07CAD C DAP Parameter Register(Default Value: 0x2C2C2828)

| Offset: 0x07C | | | Register Name: AC_ADC_DAP_PARA |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:30 | / | / | / |
| 29:24 | R/W | 0x2C | ADAP_LTARG_SET. Left channel target level setting (-1dB -- -30dB). (6.0format 2s component) |
| 23:22 | / | / | / |
| 21:16 | R/W | 0x2C | ADAP_RTARG_SET. Right channel target level setting (-1dB -- -30dB). (6.0format 2s component) |
| 15:8 | R/W | 0x28 | ADAP_LGAIN_MAX. Left channel max gain setting (0-40dB). (7.1format 2s component) |
| 7:0 | R/W | 0x28 | ADAP_RGAIN_MAX. Right channel max gain setting (0-40dB). (7.1format 2s component) |

4.14.5.19. 0x080 ADC DAP Left Average Coef Register(Default Value: 0x00051EB8)

| Offset: 0x080 | | | Register Name: AC_ADC_DAP_LAC |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:27 | / | / | / |
| 26:0 | R/W | 0x00051EB8 | ADAP_LAC. Average level coefficient setting(3.24format 2s component) |

4.14.5.20. 0x084 ADC DAP Left Decay & Attack Time Register(Default Value: 0x0000001F)

| Offset: 0x084 | | | Register Name: AC_ADC_DAP_LDAT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30:16 | R/W | 0x0000 | ADAP_LATT_SET Left attack time coefficient setting 0000 : 1x32/fs |

| | | | |
|------|-----|-------------------------|--|
| | | | 0001 : 2x32/fs ----- 7FFF : 215 x32/fs T=(n+1)*32*fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time. |
| 15 | / | / | / |
| 14:0 | R/W | 0x001F (32x32fs) | ADAP_LDEC_SET Left decay time coefficient setting 0000 : 1x32/fs 0001 : 2x32/fs ----- 7FFF : 215 x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time. |

4.14.5.21. 0x088 ADC DAP Right Average Coef Register(Default Value: 0x00051EB8)

| Offset: 0x088 | | | Register Name: AC_ADC_DAP_RAC |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:27 | / | / | / |
| 26:0 | R/W | 0x0051EB8 | ADAP_RAC. Average level coefficient setting(3.24format) |

4.14.5.22. 0x08C ADC DAP Right Decay & Attack Time Register(Default Value: 0x0000001F)

| Offset: 0x8C | | | Register Name: AC_ADC_DAP_RDAT |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30:16 | R/W | 0x0000 | ADAP_RATT_SET. Right attack time coefficient setting 0000 : 1x32/fs 0001 : 2x32/fs ----- 7FFF : 215 x32/fs T=(n+1)*32/fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time. |
| 15 | / | / | / |
| 14:0 | R/W | 0x001F | ADAP_RDEC_SET Right decay time coefficient setting 0000 : 1x32/fs 0001 : 2x32/fs ----- 7FFF : 215x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time. |

4.14.5.23. 0x090 ADC DAP HPF Coef Register(Default Value: 0x00FFAC1)

| Offset: 0x090 | | | Register Name: AC_ADC_DAP_HPFC |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:27 | / | / | / |
| 26:0 | R/W | 0x00FFAC1 | ADAP_HPFC. HPF coefficient setting (3.24format) |

4.14.5.24. 0x094 ADC DAP Left Input Signal Low Average Coef Register(Default Value: 0x00051EB8)

| Offset: 0x094 | | | Register Name: AC_ADC_DAP_LINAC |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:27 | / | / | / |
| 26:0 | R/W | 0x00051EB8 | ADAP_LINAC Left input signal average filter coefficient to check noise or not (the coefficient is 3.24 format 2s complement) always the same as the left output signal average filter's |

4.14.5.25. 0x098 ADC DAP Right Input Signal Low Average Coef Register(Default Value: 0x00051EB8)

| Offset: 0x098 | | | Register Name: AC_ADC_DAP_RNAC |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:27 | / | / | / |
| 26:0 | R/W | 0x00051EB8 | ADAP_RINAC Right input signal average filter coefficient to check noise or not (the coefficient is 3.24 format 2s complement) always the same as the left output signal average filter's |

4.14.5.26. 0x09C ADC DAP Optimum Register(Default Value: 0x00000000)

| Offset: 0x09C | | | Register Name: AC_ADC_DAP_OPT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:11 | / | / | / |
| 10 | R/W | 0x0 | Left energy default value setting(include the input and output) 0 : min 1 : max |
| 9 :8 | R/W | 0x0 | Left channel gain hysteresis setting. The different between target level and the signal level must larger than the hysteresis when the gain change. 00 : 0.4375db 01 : 0.9375db 10 : 1.9375db 11 : 3db |
| 7:3 | / | / | / |
| 5 | R/W | 0x0 | The input signal average filter coefficient setting 0 : is the reg94/reg98 1 : is the reg80/reg88; |
| 4 | R/W | 0x0 | AGC output when the channel in noise state |

| | | | |
|------|-----|-----|--|
| | | | 0 : output is zero 1 : output is the input data |
| 3 | / | / | / |
| 2 | R/W | 0x0 | Right energy default value setting(include the input and output) 0 : min 1 : max |
| 1 :0 | R/W | 0x0 | Right channel gain hysteresis setting. The different between target level and the signal level must larger than the hysteresis when the gain change. 00 : 0.4375db 01 : 0.9375db 10 : 1.9375db 11 : 3db |

4.14.5.27. 0x100 DAC DRC High HPF Coef Register(Default Value: 0x000000FF)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x100 | | | Register Name: AC_DAC_DRC_HHPFC |
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0xFF | HPF coefficient setting and the data is 3.24 format. |

4.14.5.28. 0x104 DAC DRC Low HPF Coef Register(Default Value: 0x0000FAC1)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x104 | | | Register Name: AC_DAC_DRC_LHPFC |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xFAC1 | HPF coefficient setting and the data is 3.24 format. |

4.14.5.29. 0x108 DAC DRC Control Register(Default Value: 0x00000080)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x108 | | | Register Name: AC_DAC_DRC_CTRL |
| Bit | R/W | Default/Hex | Description |
| 15 | R | 0 | DRC delay buffer data output state when drc delay function is enable and the drc function disable. After disable drc function and this bit go to 0, the user should write the drc delay function bit to 0; 0 : not complete 1 : is complete |
| 14:10 | / | / | / |
| 13:8 | R/W | 0 | Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ----- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disable, the signal delay time is unused. |
| 7 | R/W | 0x1 | The delay buffer use or not when the drc disable and the drc buffer data output completely |

| | | | |
|---|-----|-----|--|
| | | | 0 : don't use the buffer 1 : use the buffer |
| 6 | R/W | 0x0 | DRC gain max limit enable 0 : disable 1 : enable |
| 5 | R/W | 0x0 | DRC gain min limit enable. when this fuction enable, it will overwrite the noise detect fuction. 0 : disable 1 : enable |
| 4 | R/W | 0x0 | Control the drc to detect noise when ET enable 0 : disable 1 : enable |
| 3 | R/W | 0x0 | Signal function Select 0 : RMS filter 1 : Peak filter When Signal function Select Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused. (AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT) |
| 2 | R/W | 0x0 | Delay function enable 0 : disable 1 : enable When the Delay function enable is disable, the Signal delay time is unused. |
| 1 | R/W | 0x0 | DRC LT enable 0 : disable 1 : enable When the DRC LT is disable the LT, KI and OPL parameter is unused. |
| 0 | R/W | 0x0 | DRC ET enable 0 : disable 1 : enable When the DRC ET is disable the ET, Ke and OPE parameter is unused. |

4.14.5.30. 0x10C DAC DRC Left Peak Filter High Attack Time Coef Register(Default Value: 0x0000000B)

| Offset: 0x10C | | | Register Name: AC_DAC_DRC_LPFHAT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x000B | The left peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/ta)$. The format is 3.24. (1ms) |

4.14.5.31. 0x110 DAC DRC Left Peak Filter Low Attack Time Coef Register(Default Value: 0x000077BF)

| Offset: 0x110 | | | Register Name: AC_DAC_DRC_LPFLAT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x77BF | The left peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/ta)$. The format is 3.24. (1ms) |

4.14.5.32. 0x114 DAC DRC Right Peak Filter High Attack Time Coef Register(Default Value: 0x0000000B)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x114 | | | Register Name: AC_DAC_DRC_RPFHAT |
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x000B | The left peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2Ts/ta)$. The format is 3.24. (1ms) |

4.14.5.33. 0x118 DAC DRC Peak Filter Low Attack Time Coef Register(Default Value: 0x000077BF)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x118 | | | Register Name: AC_DAC_DRC_RPFLAT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x77BF | The left peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2Ts/ta)$. The format is 3.24. (1ms) |

4.14.5.34. 0x11C DAC DRC Left Peak Filter High Release Time Coef Register(Default Value: 0x000000FF)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x11C | | | Register Name: AC_DAC_DRC_LPFHRT |
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x00FF | The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms) |

4.14.5.35. 0x120 DAC DRC Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000E1F8)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x120 | | | Register Name: AC_DAC_DRC_LPFLRT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xE1F8 | The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms) |

4.14.5.36. 0x124 DAC DRC Right Peak filter High Release Time Coef Register(Default Value: 0x000000FF)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x124 | | | Register Name: AC_DAC_DRC_RPFHRT |
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x00FF | The left peak filter attack time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms) |

4.14.5.37. 0x128 DAC DRC Right Peak filter Low Release Time Coef Register(Default Value: 0x0000E1F8)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x128 | | | Register Name: AC_DAC_DRC_RPFLRT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xE1F8 | The left peak filter release time parameter setting, which determine by the equation that $AT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms) |

4.14.5.38. 0x12C DAC DRC Left RMS Filter High Coef Register(Default Value: 0x00000001)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x12C | | | Register Name: AC_DAC_DRC_LRMSHAT |
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0001 | The left RMS filter average time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/\tau_{av})$. The format is 3.24. (10ms) |

4.14.5.39. 0x130 DAC DRC Left RMS Filter Low Coef Register(Default Value: 0x00002BAF)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x130 | | | Register Name: AC_DAC_DRC_LRMSLAT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x2BAF | The left RMS filter average time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/\tau_{av})$. The format is 3.24. (10ms) |

4.14.5.40. 0x134 DAC DRC Right RMS Filter High Coef Register(Default Value: 0x00000001)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x134 | | | Register Name: AC_DAC_DRC_RRMSHAT |
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0001 | The right RMS filter average time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/\tau_{av})$. The format is 3.24. (10ms) |

4.14.5.41. 0x138 DAC DRC Right RMS Filter Low Coef Register(Default Value: 0x00002BAF)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x138 | | | Register Name: AC_DAC_DRC_RRMSLAT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x2BAF | The right RMS filter average time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/\tau_{av})$. The format is 3.24. (10ms) |

4.14.5.42. 0x13C DAC DRC Compressor Theshold High Setting Register(Default Value: 0x000006A4)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x13C | | | Register Name: AC_DAC_DRC_HCT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x06A4 | The compressor threshold setting, which set by the equation that $CT_{in} = -CT/6.0206$. The format is 8.24 (-40dB) |

4.14.5.43. 0x140 DAC DRC Compressor Slope High Setting Register(Default Value: 0x0000D3C0)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x140 | | | Register Name: AC_DAC_DRC_LCT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xD3C0 | The compressor threshold setting, which set by the equation that $CT_{in} = -CT/6.0206$. The format is 8.24 (-40dB) |

4.14.5.44. 0x144 DAC DRC Compressor Slope High Setting Register(Default Value: 0x00000080)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x144 | | | Register Name: AC_DAC_DRC_HKC |
| Bit | R/W | Default/Hex | Description |
| 15:13 | / | / | / |
| 13:0 | R/W | 0x0080 | The slope of the compressor which determine by the equation that $K_c = 1/R$, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1) |

4.14.5.45. 0x148 DAC DRC Compressor Slope Low Setting Register(Default Value: 0x00000000)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x148 | | | Register Name: AC_DAC_DRC_LKC |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0000 | The slope of the compressor which determine by the equation that $K_c = 1/R$, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1) |

4.14.5.46. 0x14C DAC DRC Compressor High Output at Compressor Threshold Register(Default Value: 0x0000F95B)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x14C | | | Register Name: AC_DAC_DRC_HOPC |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xF95B | The output of the compressor which determine by the equation $-OPC/6.0206$ The format is 8.24 (-40dB) |

4.14.5.47. 0x150 DAC DRC Compressor Low Output at Compressor Threshold Register(Default Value: 0x00002C3F)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x150 | | | Register Name: AC_DAC_DRC_LOPC |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x2C3F | The output of the compressor which determine by the equation $OPC/6.0206$ The format is 8.24 (-40dB) |

4.14.5.48. 0x154 DAC DRC Limiter Theshold High Setting Register(Default Value: 0x000001A9)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x154 | | | Register Name: AC_DAC_DRC_HLT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x01A9 | The limiter threshold setting, which set by the equation that $LT_{in} = -LT/6.0206$, The format is 8.24. (-10dB) |

4.14.5.49. 0x158 DAC DRC Limiter Theshold Low Setting Register(Default Value: 0x000034F0)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x158 | | | Register Name: AC_DAC_DRC_LLT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x34F0 | The limiter threshold setting, which set by the equation that $LT_{in} = -LT/6.0206$, |

| | | | |
|--|--|--|-----------------------------|
| | | | The format is 8.24. (-10dB) |
|--|--|--|-----------------------------|

4.14.5.50. 0x15C DAC DRC Limiter Slope High Setting Register(Default Value: 0x00000005)

| Offset: 0x15C | | | Register Name: AC_DAC_DRC_HKI |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 13:0 | R/W | 0x0005 | The slope of the limiter which determine by the equation that $KI = 1/R$, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1) |

4.14.5.51. 0x160 DAC DRC Limiter Slope Low Setting Register(Default Value: 0x1EB8)

| Offset: 0x160 | | | Register Name: AC_DAC_DRC_LKI |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x1EB8 | The slope of the limiter which determine by the equation that $KI = 1/R$, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1) |

4.14.5.52. 0x164 DAC DRC Limiter High Output at Limiter Threshold(Default Value: 0x0000FBD8)

| Offset: 0x164 | | | Register Name: AC_DAC_DRC_HOPL |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xFBD8 | The output of the limiter which determine by equation $OPT/6.0206$. The format is 8.24 (-25dB) |

4.14.5.53. 0x168 DAC DRC Limiter Low Output at Limiter Threshold(Default Value: 0x0000FBA7)

| Offset: 0x168 | | | Register Name: AC_DAC_DRC_LOPL |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xFBA7 | The output of the limiter which determine by equation $OPT/6.0206$. The format is 8.24 (-25dB) |

4.14.5.54. 0x16C DAC DRC Expander Theshold High Setting Register(Default Value: 0x0000BA0)

| Offset: 0x16C | | | Register Name: AC_DAC_DRC_HET |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0BA0 | The expander threshold setting, which set by the equation that $ETin = -ET/6.0206$, The format is 8.24. (-70dB) |

4.14.5.55. 0x170 DAC DRC Expander Theshold Low Setting Register(Default Value: 0x00007291)

| Offset: 0x170 | | | Register Name: AC_DAC_DRC_LET |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x7291 | The expander threshold setting, which set by the equation that $ETin =$ |

| | | | |
|--|--|--|---|
| | | | -ET/6.0206, The format is 8.24. (-70dB) |
|--|--|--|---|

4.14.5.56. 0x174 DAC DRC Expander Slope High Setting Register(Default Value: 0x00000500)

| Offset: 0x174 | | | Register Name: AC_DAC_DRC_HKE |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:14 | / | / | / |
| 13:0 | R/W | 0x0500 | The slope of the expander which determine by the equation that $K_e = 1/R$, there, R is the ratio of the expander, which always is interger and the k_e must larger than 50. The format is 8.24. (1:5) |

4.14.5.57. 0x178 DAC DRC Expander Slope Low Setting Register(Default Value: 0x00000000)

| Offset: 0x178 | | | Register Name: AC_DAC_DRC_LKE |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0000 | The slope of the expander which determine by the equation that $K_e = 1/R$, there, R is the ratio of the expander, which always is interger and the k_e must larger than 50. The format is 8.24. (1:5) |

4.14.5.58. 0x17C DAC DRC Expander High Output at Expander Threshold(Default Value: 0xF45F)

| Offset: 0x17C | | | Register Name: AC_DAC_DRC_HOPE |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xF45F | The output of the expander which determine by equation $OPE/6.0206$. The format is 8.24 (-70dB) |

4.14.5.59. 0x180 DAC DRC Expander Low Output at Expander Threshold(Default Value: 0x00008D6E)

| Offset: 0x180 | | | Register Name: AC_DAC_DRC_LOPE |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x8D6E | The output of the expander which determine by equation $OPE/6.0206$. The format is 8.24 (-70dB) |

4.14.5.60. 0x184 DAC DRC Linear Slope High Setting Register(Default Value: 0x00000100)

| Offset: 0x184 | | | Register Name: AC_DAC_DRC_HKN |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:14 | / | / | / |
| 13:0 | R/W | 0x0100 | The slope of the linear which determine by the equation that $K_n = 1/R$, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1) |

4.14.5.61. 0x188 DAC DRC Linear Slope Low Setting Register(Default Value: 0x00000000)

| Offset: 0x188 | | | Register Name: AC_DAC_DRC_LKN |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0000 | The slope of the linear which determine by the equation that $K_n = 1/R$, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1) |

4.14.5.62. 0x18C DAC DRC Smooth filter Gain High Attack Time Coef Register(Default Value: 0x00000002)

| Offset: 0x18C | | | Register Name: AC_DAC_DRC_SFHAT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0002 | The smooth filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (5ms) |

4.14.5.63. 0x190 DAC DRC Smooth filter Gain Low Attack Time Coef Register(Default Value: 0x00005600)

| Offset: 0x190 | | | Register Name: AC_DAC_DRC_SFLAT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x5600 | The smooth filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (5ms) |

4.14.5.64. 0x194 DAC DRC Smooth filter Gain High Release Time Coef Register(Default Value: 0x00000000)

| Offset: 0x194 | | | Register Name: AC_DAC_DRC_SFHRT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0000 | The gain smooth filter release time parameter setting, which determine by the equation that $RT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (200ms) |

4.14.5.65. 0x198 DAC DRC Smooth filter Gain Low Release Time Coef Register(Default Value: 0x00000F04)

| Offset: 0x198 | | | Register Name: AC_DAC_DRC_SFLRT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0F04 | The gain smooth filter release time parameter setting, which determine by the equation that $RT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (200ms) |

4.14.5.66. 0x19C DAC DRC MAX Gain High Setting Register(Default Value: 0x0000FE56)

| Offset: 0x19C | | | Register Name: AC_DAC_DRC_MXGHS |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xFE56 | The max gain setting which determine by equation $MXG/6.0206$. The format is 8.24 and must $-20dB < MXG < 30dB$ (-10dB) |

4.14.5.67. 0x1A0 DAC DRC MAX Gain Low Setting Register(Default Value: 0x0000CB0F)

| Offset: 0x1A0 | | | Register Name: AC_DAC_DRC_MXGLS |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xCB0F | The max gain setting which determine by equation $MXG/6.0206$. The format is 8.24 and must $-20dB < MXG < 30dB$ (-10dB) |

4.14.5.68. 0x1A4 DAC DRC MIN Gain High Setting Register(Default Value: 0x0000_F95B)

| Offset: 0x1A4 | | | Register Name: AC_DAC_DRC_MNGHS |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xF95B | The min gain setting which determine by equation $MXG/6.0206$. The format is 8.24 and must $-60dB \leq MNG \leq -30dB$ (-40dB) |

4.14.5.69. 0x1A8 DAC DRC MIN Gain Low Setting Register(Default Value: 0x00002C3F)

| Offset: 0x1A8 | | | Register Name: AC_DAC_DRC_MNGLS |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x2C3F | The min gain setting which determine by equation $MNG/6.0206$. The format is 8.24 and must $-60dB \leq MNG \leq -30dB$ (-40dB) |

4.14.5.70. 0x1AC DAC DRC Expander Smooth Time High Coef Register(Default Value: 0x00000000)

| Offset: 0x1AC | | | Register Name: AC_DAC_DRC_EPSHC |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 11:0 | R/W | 0x0000 | The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that $RT = 1 - \exp(-2.2Ts/tr)$. The format is 3.24. (30ms) |

4.14.5.71. 0x1B0 DAC DRC Expander Smooth Time Low Coef Register(Default Value: 0x0000640C)

| Offset: 0x1B0 | | | Register Name: AC_DAC_DRC_EPSLC |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x640C | The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that $RT = 1 - \exp(-2.2Ts/tr)$. The format is 3.24. (30ms) |

4.14.5.72. 0x1B8 DAC DRC HPF Gain High Coef Register(Default Value: 0x00000100)

| Offset: 0x1B8 | | | Register Name: AC_DAC_DRC_HPFHGAIN |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x100 | The gain of the hpf coefficient setting which format is 3.24.(gain = 1) |

4.14.5.73. 0x1BC DAC DRC HPF Gain Low Coef Register(Default Value: 0x00000000)

| Offset: 0x1BC | | | Register Name: AC_DAC_DRC_HPFLGAIN |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0000 | The gain of the hpf coefficient setting which format is 3.24.(gain = 1) |

4.14.5.74. 0x200 ADC DRC High HPF Coef Register(Default Value: 0x000000FF)

| Offset: 0x200 | | | Register Name: AC_ADC_DRC_HHPFC |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0xFF | HPF coefficient setting and the data is 3.24 format. |

4.14.5.75. 0x204 ADC DRC Low HPF Coef Register(Default Value: 0x0000FAC1)

| Offset: 0x204 | | | Register Name: AC_ADC_DRC_LHPFC |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xFAC1 | HPF coefficient setting and the data is 3.24 format. |

4.14.5.76. 0x208 ADC DRC Control Register(Default Value: 0x00000080)

| Offset: 0x208 | | | Register Name: AC_ADC_DRC_CTRL |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15 | R | 0 | DRC delay buffer data output state when drc delay function is enable and the drc function disable. After disable drc function and this bit go to 0, the user should write the drc delay function bit to 0; 0 : not complete 1 : is complete |
| 14:10 | / | / | / |
| 13:8 | R/W | 0 | Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ----- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disable, the signal delay time is unused. |
| 7 | R/W | 0x1 | The delay buffer use or not when the drc disable and the drc buffer data output completely 0 : don't use the buffer 1 : use the buffer |
| 6 | R/W | 0x0 | DRC gain max limit enable 0 : disable 1 : enable |
| 5 | R/W | 0x0 | DRC gain min limit enable. when this function enable, it will overwrite the noise detect function. 0 : disable |

| | | | |
|---|-----|-----|--|
| | | | 1 : enable |
| 4 | R/W | 0x0 | Control the drc to detect noise when ET enable 0 : disable 1 : enable |
| 3 | R/W | 0x0 | Signal function Select 0 : RMS filter 1 : Peak filter When Signal function Select Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused. (AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT) |
| 2 | R/W | 0x0 | Delay function enable 0 : disable 1 : enable When the Delay function enable is disable, the Signal delay time is unused. |
| 1 | R/W | 0x0 | DRC LT enable 0 : disable 1 : enable When the DRC LT is disable the LT, KI and OPL parameter is unused. |
| 0 | R/W | 0x0 | DRC ET enable 0 : disable 1 : enable When the DRC ET is disable the ET, Ke and OPE parameter is unused. |

4.14.5.77. 0x20C ADC DRC Left Peak Filter High Attack Time Coef Register(Default Value: 0x0000000B)

| Offset: 0x20C | | | Register Name: AC_ADC_DRC_LPFHAT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x000B | The left peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2Ts/ta)$. The format is 3.24. (1ms) |

4.14.5.78. 0x210 ADC DRC Left Peak Filter Low Attack Time Coef Register(Default Value: 0x000077BF)

| Offset: 0x210 | | | Register Name: AC_ADC_DRC_LPFLAT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x77BF | The left peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2Ts/ta)$. The format is 3.24. (1ms) |

4.14.5.79. 0x214 ADC DRC Right Peak Filter High Attack Time Coef Register(Default Value: 0x0000000B)

| Offset: 0x214 | | | Register Name: AC_ADC_DRC_RPFHAT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x000B | The left peak filter attack time parameter setting, which determine by the |

| | | | |
|--|--|--|---|
| | | | equation that $AT = 1 - \exp(-2.2T_s/ta)$. The format is 3.24. (1ms) |
|--|--|--|---|

4.14.5.80. 0x218 ADC DRC Peak Filter Low Attack Time Coef Register(Default Value: 0x000077BF)

| Offset: 0x218 | | | Register Name: AC_ADC_DRC_RPFLAT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x77BF | The left peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/ta)$. The format is 3.24. (1ms) |

4.14.5.81. 0x21C ADC DRC Left Peak Filter High Release Time Coef Register(Default Value: 0x000000FF)

| Offset: 0x21C | | | Register Name: AC_ADC_DRC_LPFHRT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x00FF | The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2T_s/tr)$. The format is 3.24. (100ms) |

4.14.5.82. 0x220 ADC DRC Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000E1F8)

| Offset: 0x220 | | | Register Name: AC_ADC_DRC_LPFLRT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xE1F8 | The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2T_s/tr)$. The format is 3.24. (100ms) |

4.14.5.83. 0x224 ADC DRC Right Peak filter High Release Time Coef Register(Default Value: 0x000000FF)

| Offset: 0x224 | | | Register Name: AC_ADC_DRC_RPFHRT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x00FF | The left peak filter attack time parameter setting, which determine by the equation that $RT = \exp(-2.2T_s/tr)$. The format is 3.24. (100ms) |

4.14.5.84. 0x228 ADC DRC Right Peak filter Low Release Time Coef Register(Default Value: 0x0000E1F8)

| Offset: 0x228 | | | Register Name: AC_ADC_DRC_RPFLRT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xE1F8 | The left peak filter release time parameter setting, which determine by the equation that $AT = \exp(-2.2T_s/tr)$. The format is 3.24. (100ms) |

4.14.5.85. 0x22C ADC DRC Left RMS Filter High Coef Register(Default Value: 0x00000001)

| Offset: 0x22C | | | Register Name: AC_ADC_DRC_LRMSHAT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0001 | The left RMS filter average time parameter setting, which determine by the |

| | | | |
|--|--|--|--|
| | | | equation that $AT = 1 - \exp(-2.2T_s/t_{av})$. The format is 3.24. (10ms) |
|--|--|--|--|

4.14.5.86. 0x230 ADC DRC Left RMS Filter Low Coef Register(Default Value: 0x00002BAF)

| Offset: 0x230 | | | Register Name: AC_ADC_DRC_LRMSLAT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x2BAF | The left RMS filter average time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/t_{av})$. The format is 3.24. (10ms) |

4.14.5.87. 0x234 ADC DRC Right RMS Filter High Coef Register(Default Value: 0x00000001)

| Offset: 0x234 | | | Register Name: AC_ADC_DRC_RRMSHAT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0001 | The right RMS filter average time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/t_{av})$. The format is 3.24. (10ms) |

4.14.5.88. 0x238 ADC DRC Right RMS Filter Low Coef Register(Default Value: 0x00002BAF)

| Offset: 0x238 | | | Register Name: AC_ADC_DRC_RRMSLAT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x2BAF | The right RMS filter average time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/t_{av})$. The format is 3.24. (10ms) |

4.14.5.89. 0x23C ADC DRC Compressor Theshold High Setting Register(Default Value: 0x000006A4)

| Offset: 0x23C | | | Register Name: AC_ADC_DRC_HCT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x06A4 | The compressor threshold setting, which set by the equation that $CT_{in} = -CT/6.0206$. The format is 8.24 (-40dB) |

4.14.5.90. 0x240 ADC DRC Compressor Slope High Setting Register(Default Value: 0x0000D3C0)

| Offset: 0x240 | | | Register Name: AC_ADC_DRC_LCT |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xD3C0 | The compressor threshold setting, which set by the equation that $CT_{in} = -CT/6.0206$. The format is 8.24 (-40dB) |

4.14.5.91. 0x244 ADC DRC Compressor Slope High Setting Register(Default Value: 0x00000080)

| Offset: 0x244 | | | Register Name: AC_ADC_DRC_HKC |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:13 | / | / | / |
| 13:0 | R/W | 0x0080 | The slope of the compressor which determine by the equation that $K_c = 1/R$, |

| | | | |
|--|--|--|--|
| | | | there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1) |
|--|--|--|--|

4.14.5.92. 0x248 ADC DRC Compressor Slope Low Setting Register(Default Value: 0x00000000)

| Offset: 0x248 | | | Register Name: AC_ADC_DRC_LKC |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0000 | The slope of the compressor which determine by the equation that $K_c = 1/R$, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1) |

4.14.5.93. 0x24C ADC DRC Compressor High Output at Compressor Threshold Register(Default Value: 0x0000F95B)

| Offset: 0x24C | | | Register Name: AC_ADC_DRC_HOPC |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xF95B | The output of the compressor which determine by the equation $-OPC/6.0206$ The format is 8.24 (-40dB) |

4.14.5.94. 0x250 ADC DRC Compressor Low Output at Compressor Threshold Register(Default Value: 0x00002C3F)

| Offset: 0x250 | | | Register Name: AC_ADC_DRC_LOPC |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x2C3F | The output of the compressor which determine by the equation $OPC/6.0206$ The format is 8.24 (-40dB) |

4.14.5.95. 0x254 ADC DRC Limiter Theshold High Setting Register(Default Value: 0x000001A9)

| Offset: 0x254 | | | Register Name: AC_ADC_DRC_HLT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x01A9 | The limiter threshold setting, which set by the equation that $LT_{in} = -LT/6.0206$, The format is 8.24. (-10dB) |

4.14.5.96. 0x258 ADC DRC Limiter Theshold Low Setting Register(Default Value: 0x000034F0)

| Offset: 0x258 | | | Register Name: AC_ADC_DRC_LLT |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x34F0 | The limiter threshold setting, which set by the equation that $LT_{in} = -LT/6.0206$, The format is 8.24. (-10dB) |

4.14.5.97. 0x25C ADC DRC Limiter Slope High Setting Register(Default Value: 0x00000005)

| Offset: 0x25C | | | Register Name: AC_ADC_DRC_HKI |
|---------------|-----|-------------|--------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |

| | | | |
|------|-----|--------|--|
| 13:0 | R/W | 0x0005 | The slope of the limiter which determine by the equation that $KI = 1/R$, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1) |
|------|-----|--------|--|

4.14.5.98. 0x260 ADC DRC Limiter Slope Low Setting Register(Default Value: 0x1EB8)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x260 | | | Register Name: AC_ADC_DRC_LKI |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x1EB8 | The slope of the limiter which determine by the equation that $KI = 1/R$, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1) |

4.14.5.99. 0x264 ADC DRC Limiter High Output at Limiter Threshold(Default Value: 0x0000FBD8)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x264 | | | Register Name: AC_ADC_DRC_HOPL |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xFBD8 | The output of the limiter which determine by equation $OPT/6.0206$. The format is 8.24 (-25dB) |

4.14.5.100. 0x268 ADC DRC Limiter Low Output at Limiter Threshold(Default Value: 0x0000FBA7)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x268 | | | Register Name: AC_ADC_DRC_LOPL |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xFBA7 | The output of the limiter which determine by equation $OPT/6.0206$. The format is 8.24 (-25dB) |

4.14.5.101. 0x26C ADC DRC Expander Theshold High Setting Register(Default Value: 0x0000BA0)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x26C | | | Register Name: AC_ADC_DRC_HET |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0BA0 | The expander threshold setting, which set by the equation that $ETin = -ET/6.0206$, The format is 8.24. (-70dB) |

4.14.5.102. 0x270 ADC DRC Expander Theshold Low Setting Register(Default Value: 0x00007291)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x270 | | | Register Name: AC_ADC_DRC_LET |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x7291 | The expander threshold setting, which set by the equation that $ETin = -ET/6.0206$, The format is 8.24. (-70dB) |

4.14.5.103. 0x274 ADC DRC Expander Slope High Setting Register(Default Value: 0x00000500)

| | | | |
|---------------|-----|-------------|--------------------------------------|
| Offset: 0x274 | | | Register Name: AC_ADC_DRC_HKE |
| Bit | R/W | Default/Hex | Description |
| 15:14 | / | / | / |

| | | | |
|------|-----|--------|--|
| 13:0 | R/W | 0x0500 | The slope of the expander which determine by the equation that $K_e = 1/R$, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (1:5) |
|------|-----|--------|--|

4.14.5.104. 0x278 ADC DRC Expander Slope Low Setting Register(Default Value: 0x00000000)

| Offset: 0x278 | | | Register Name: AC_ADC_DRC_LKE |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0000 | The slope of the expander which determine by the equation that $K_e = 1/R$, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (1:5) |

4.14.5.105. 0x27C ADC DRC Expander High Output at Expander Threshold(Default Value: 0xF45F)

| Offset: 0x27C | | | Register Name: AC_ADC_DRC_HOPE |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xF45F | The output of the expander which determine by equation $OPE/6.0206$. The format is 8.24 (-70dB) |

4.14.5.106. 0x280 ADC DRC Expander Low Output at Expander Threshold(Default Value: 0x00008D6E)

| Offset: 0x280 | | | Register Name: AC_ADC_DRC_LOPE |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x8D6E | The output of the expander which determine by equation $OPE/6.0206$. The format is 8.24 (-70dB) |

4.14.5.107. 0x284 ADC DRC Linear Slope High Setting Register(Default Value: 0x00000100)

| Offset: 0x284 | | | Register Name: AC_ADC_DRC_HKN |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:14 | / | / | / |
| 13:0 | R/W | 0x0100 | The slope of the linear which determine by the equation that $K_n = 1/R$, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1) |

4.14.5.108. 0x288 ADC DRC Linear Slope Low Setting Register(Default Value: 0x00000000)

| Offset: 0x288 | | | Register Name: AC_ADC_DRC_LKN |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0000 | The slope of the linear which determine by the equation that $K_n = 1/R$, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1) |

4.14.5.109. 0x28C ADC DRC Smooth filter Gain High Attack Time Coef Register(Default Value: 0x00000002)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x28C | | | Register Name: AC_ADC_DRC_SFHAT |
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0002 | The smooth filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (5ms) |

4.14.5.110. 0x290 ADC DRC Smooth filter Gain Low Attack Time Coef Register(Default Value: 0x00005600)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x290 | | | Register Name: AC_ADC_DRC_SFLAT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x5600 | The smooth filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (5ms) |

4.14.5.111. 0x294 ADC DRC Smooth filter Gain High Release Time Coef Register(Default Value: 0x00000000)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x294 | | | Register Name: AC_ADC_DRC_SFHRT |
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0000 | The gain smooth filter release time parameter setting, which determine by the equation that $RT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (200ms) |

4.14.5.112. 0x298 ADC DRC Smooth filter Gain Low Release Time Coef Register(Default Value: 0x00000F04)

| | | | |
|---------------|-----|-------------|---|
| Offset: 0x298 | | | Register Name: AC_ADC_DRC_SFLRT |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0F04 | The gain smooth filter release time parameter setting, which determine by the equation that $RT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (200ms) |

4.14.5.113. 0x29C ADC DRC MAX Gain High Setting Register(Default Value: 0x0000FE56)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x29C | | | Register Name: AC_ADC_DRC_MXGHS |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xFE56 | The max gain setting which determine by equation $MXG/6.0206$. The format is 8.24 and must $-20dB < MXG < 30dB (-10dB)$ |

4.14.5.114. 0x2A0 ADC DRC MAX Gain Low Setting Register(Default Value: 0x0000CB0F)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x2A0 | | | Register Name: AC_ADC_DRC_MXGLS |
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xCB0F | The max gain setting which determine by equation $MXG/6.0206$. The format is 8.24 and must $-20dB < MXG < 30dB (-10dB)$ |

4.14.5.115. 0x2A4 ADC DRC MIN Gain High Setting Register(Default Value: 0x0000F95B)

| Offset: 0x2A4 | | | Register Name: AC_ADC_DRC_MNGHS |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0xF95B | The min gain setting which determine by equation $MXG/6.0206$. The format is 8.24 and must $-60dB \leq MNG \leq -30dB$ (-40dB) |

4.14.5.116. 0x2A8 ADC DRC MIN Gain Low Setting Register(Default Value: 0x00002C3F)

| Offset: 0x2A8 | | | Register Name: AC_ADC_DRC_MNGLS |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x2C3F | The min gain setting which determine by equation $MNG/6.0206$. The format is 8.24 and must $-60dB \leq MNG \leq -30dB$ (-40dB) |

4.14.5.117. 0x2AC ADC DAP Expander Smooth Time High Coef Register(Default Value: 0x00000000)

| Offset: 0x2AC | | | Register Name: AC_ADC_DRC_EPSHC |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 11:0 | R/W | 0x0000 | The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that $RT = 1 - \exp(-2.2Ts/tr)$. The format is 3.24. (30ms) |

4.14.5.118. 0x2B0 ADC DRC Expander Smooth Time Low Coef Register (Default Value: 0x0000640C)

| Offset: 0x2B0 | | | Register Name: AC_ADC_DRC_EPSLC |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x640C | The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that $RT = 1 - \exp(-2.2Ts/tr)$. The format is 3.24. (30ms) |

4.14.5.119. 0x2B8 ADC DRC HPF Gain High(Default Value: 0x00000100)

| Offset: 0x2B8 | | | Register Name: AC_ADC_DRC_HPFHGAIN |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x100 | The gain of the hpf coefficient setting which format is 3.24.(gain = 1) |

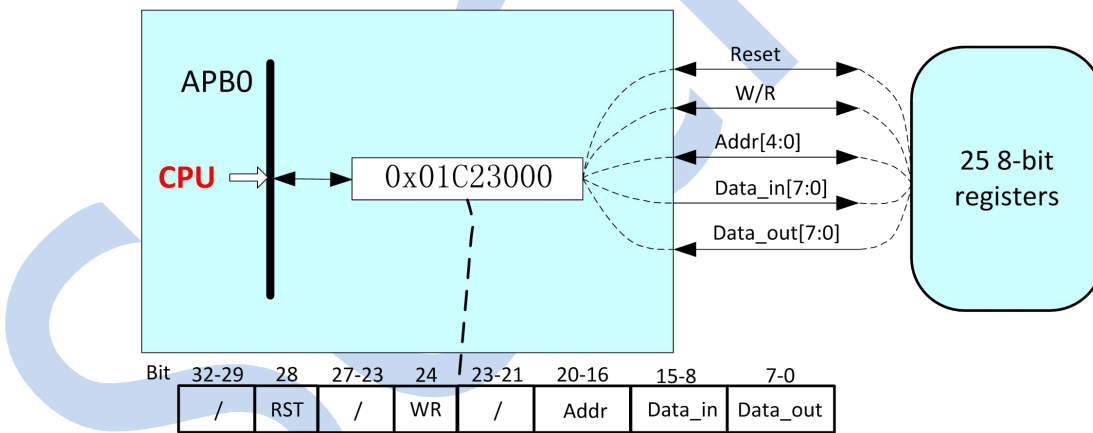
4.14.5.120. 0x2BC ADC DRC HPF Gain Low(Default Value: 0x00000000)

| Offset: 0x2BC | | | Register Name: AC_ADC_DRC_HPFLGAIN |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R/W | 0x0000 | The gain of the hpf coefficient setting which format is 3.24.(gain = 1) |

4.14.5.121. AC Parameter Configuration Register(Default Value: 0x1000000)

| Address: 0x400 | | | Register Name: AC_PR_CFG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28 | R/W | 0x1 | AC_PR_RST AC_PR Reset 0: Assert 1: De-assert |
| 27:25 | / | / | / |
| 24 | R/W | 0x0 | AC_PR_RW AC_PR Read Or Write 0: read 1: write |
| 23:21 | / | / | / |
| 20:16 | R/W | 0x0 | AC_PR_ADDR AC_PR Address [4:0] |
| 15:8 | R/W | 0x0 | ADDA_PR_WDAT ADDA_PR Write Data [7:0] |
| 7:0 | R/W | 0x0 | ADDA_PR_RDAT ADDA_PR Read Data [7:0] |

Note: The address of this Register is 0x01c23000, using this register to configure the AC_PR register.
 Reset: Reset signal; ADDR[4:0] : AC_PR Address; W/R: Write/Read Enable;
 WDAT[7:0]: Write Data; RDAT[7:0]: Read Data.



4.14.5.122. 0x00 Headphone Volume Control(Default Value: 0x00)

| Offset:0x00 | | | Register Name: AC_PAG_HP |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7 | / | / | / |
| 6 | / | / | / |
| 5:0 | R/W | 0x0 | HPVOL Headphone Volume Control, (HPVOL): Total 64 level, from 0dB to -62dB, 1dB/step, mute when 000000 |

4.14.5.123. 0x01 Left Output Mixer Source Select Control Register(Default Value: 0x00)

| Offset:0x01 | | | Register Name: AC_LOMIXSC |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7 | / | / | / |
| 6:0 | R/W | 0x0 | LMIXMUTE Left Output Mixer Mute Control 0-Mute, 1-Not Mute Bit 6: MIC1 Boost Stage Bit 5: MIC2 Boost Stage Bit 4: / Bit 3: / Bit 2: LINEINL Bit 1: Left Channel DAC Bit 0: Right Channel DAC |

4.14.5.124. 0x02 Right Output Mixer Source Select Control Register(Default Value: 0x00)

| Offset:0x02 | | | Register Name: AC_ROMIXSC |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 7 | / | / | / |
| 6:0 | R/W | 0x0 | RMIXMUTE Right Output Mixer Mute Control 0-Mute, 1-Not Mute Bit 6: MIC1 Boost Stage Bit 5: MIC2 Boost Stage Bit 4: / Bit 3: / Bit 2: LINEINR Bit 1: Right Channel DAC Bit 0: Left Channel DAC |

4.14.5.125. 0x03 DAC Analog Enable and PA Source Control Register(Default Value: 0x00)

| Offset:0x03 | | | Register Name: DAC_PA_SRC |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 7 | R/W | 0x0 | DACAREN Internal Analog Right channel DAC Enable 0:Disable; 1:Enable |
| 6 | R/W | 0x0 | DACALEN Internal Analog Left channel DAC Enable 0:Disable; 1:Enable |
| 5 | R/W | 0x0 | RMIXEN Right Analog Output Mixer Enable 0:Disable; 1:Enable |
| 4 | R/W | 0x0 | LMIXEN Left Analog Output Mixer Enable 0:Disable; 1:Enable |
| 3 | R/W | 0x0 | RHPPAMUTE All input source to Right Headphone PA mute, including Right Output mixer |

| | | | |
|---|-----|-----|--|
| | | | and Internal Right channel DAC: 0:Mute, 1: Not mute |
| 2 | R/W | 0x0 | LHPPAMUTE All input source to Left Headphone PA mute, including Left Output mixer and Internal Left channel DAC: 0:Mute, 1: Not mute |
| 1 | R/W | 0x0 | RHPIS Right Headphone Power Amplifier (PA) Input Source Select 0: Right channel DAC 1: Right Analog Mixer |
| 0 | R/W | 0x0 | LHPIS Left Headphone Power Amplifier (PA) Input Source Select 0: Left channel DAC 1: Left Analog Mixer |

4.14.5.126. 0x05 Linein Gain Control Register(Default Value: 0x33)

| Offset:0x05 | | | Register Name: LINEIN_GCTR |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 7 | / | / | / |
| 6:4 | R/W | 0x3 | LINEING, (volln) LINEINL/R to L/R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB |
| 3 | / | / | / |
| 2:0 | R/W | 0x3 | / |

4.14.5.127. 0x06 MIC1 And MIC2 Gain Control Register(Default Value: 0x33)

| Offset:0x06 | | | Register Name: MIC_GCTR |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 7 | / | / | / |
| 6:4 | R/W | 0x3 | MIC1_GAIN MIC1 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB |
| 3 | / | / | / |
| 2:0 | R/W | 0x3 | MIC2G, (volm2) MIC2 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB |

4.14.5.128. 0x07 PA Enable and HP Control Register(Default Value: 0x14)

| Offset:0x07 | | | Register Name: HP_CTRL |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 7 | R/W | 0x0 | HPPAEN Right & Left Headphone Power Amplifier Enable 0-disable 1-enable |
| 6:5 | R/W | 0x0 | HPCOM_FC, HPCOM function control 00: HPCOM off & output is floating |

| | | | |
|-----|-----|-----|--|
| | | | 01: HPL inverting output 10: HPR inverting output 11: Direct driver for HPL & HPR |
| 4 | R/W | 0x1 | HPCOM output protection enable when it is set as Direct driver for HPL/R, (COMPTEN) 0: protection disable 1: protection enable |
| 3:2 | R/W | 0x1 | COS_SLOPE_CTRL COS slope time Control for Anti-pop 00:131ms; 01: 262ms; 10: 393ms; 11:524ms |
| 1 | R/W | 0x0 | LTRNMUTE, (hprisinvhpl) Left HPOUT Negative To Right HPOUT Mute 0: Mute, 1: Not mute |
| 0 | R/W | 0x0 | RTLNMUTE, (hplisinvhpr) Right HPOUT Negative To Left HPOUT Mute 0: Mute, 1: Not mute |

4.14.5.129. 0x09 Lineout Volume Control Register(Default Value: 0x40)

| Offset:0x09 | | | Register Name: LINEOUT_VOLC |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7:3 | R/W | 0x0 | LINEOUTVOL Line-out Volume Control, Total 31 level, from 0dB to -48dB, 1.5dB/step, mute when 00000 & 00001 |
| 2:0 | R/W | 0x4 | / |

4.14.5.130. 0x0A MIC2 Boost and Lineout Enable Control Register(Default Value: 0x40)

| Offset:0x0A | | | Register Name: MIC2_LINEOUT_CTRL |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7 | R/W | 0x0 | MIC2AMPEN MIC2 Boost AMP Enable 0-Disable; 1-Enable |
| 6:4 | R/W | 0x4 | MIC2BOOST MIC2 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB |
| 3 | R/W | 0x0 | Line-out Left Enable 0-disable 1-enable |
| 2 | R/W | 0x0 | Line-out Right Enable 0-disable 1-enable |
| 1 | R/W | 0x0 | Left line-out source select 0-left output mixer 1-left output mixer + right output mixer |
| 0 | R/W | 0x0 | Right line-out source select 0-right output mixer 1-left line-out, for differential output |

4.14.5.131. 0x0B BIAS and MIC1 boost(Default Value: 0x04)

| Offset:0x0B | | | Register Name: BIAS_MIC_CTRL |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 7 | R/W | 0x0 | HMICBIASEN Headset Microphone Bias enable 0: disable, 1: enable |
| 6 | R/W | 0x0 | MMICBIASEN Master Microphone Bias enable 0: disable, 1: enable |
| 5 | R/W | 0x0 | HMICADCEN Headset MIC Bias Current sensor & ADC enable 0: Current sensor & ADC disabled 1: Current sensor & ADC enabled |
| 4 | R/W | 0x1 | MIC2 Source select 0: MICIN3 1: MICIN2 |
| 3 | R/W | 0 | MIC1AMPEN MIC1 Boost AMP Enable 0-Disable; 1-Enable |
| 2:0 | R/W | 0x4 | MIC1BOOST MIC1 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB |

4.14.5.132. 0x0C Left ADC Mixer Mute Control(Default Value: 0x00)

| Offset:0x0C | | | Register Name: LADC_MIX_MUTE |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7 | / | / | / |
| 6:0 | R/W | 0x0 | LADCMIXMUTE Left ADC Mixer Mute Control: 0: Mute; 1:On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: / Bit 3: / Bit 2: LINEINL Bit 1: Left output mixer Bit 0: Right output mixer |

4.14.5.133. 0x0D Right ADC Mixer Mute Control(Default Value: 0x00)

| Offset:0x0D | | | Register Name: RADC_MIX_MUTE |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7 | / | / | / |
| 6:0 | R/W | 0x0 | RADCMIXMUTE Right ADC Mixer Mute Control: 0: Mute; 1:On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: / |

| | | | |
|--|--|--|---|
| | | | Bit 3: / Bit 2: LINEINR Bit 1: Right output mixer Bit 0: Left output mixer |
|--|--|--|---|

4.14.5.134. 0x0E PA Anti-pop time Control(Default Value: 0x04)

| Offset:0x0E | | | Register Name: PA_ANTI_POP_CTRL |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7:3 | R/W | 0x0 | / |
| 2:0 | R/W | 0x4 | PA_ANTI_POP_CTRL, (slopelengthsel) PA Anti-pop time Control 000: 131ms; 001: 262ms; 010: 393ms; 011: 524ms; 100: 655ms; 101: 786ms; 110: 786ms; 111: 1048ms; |

4.14.5.135. 0x0F ADC Analog Control Register(Default Value: 0x03)

| Offset:0x0F | | | Register Name: AC_ADC_CTRL |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7 | R/W | 0x0 | ADCREN ADC Right Channel Enable 0-Disable; 1-Enable |
| 6 | R/W | 0x0 | ADCLEN ADC Left Channel Enable 0-Disable; 1-Enable |
| 5:3 | R/W | 0x0 | / |
| 2:0 | R/W | 0x3 | ADCG ADC Input Gain Control From -4.5dB to 6dB, 1.5dB/step default is 0dB |

4.14.5.136. 0x10 OPDRV/OPCOM/OPADC Control(Default Value: 0x55)

| Offset:0x10 | | | Register Name: OPADC_CTRL |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 7:6 | R/W | 0x1 | OPDRV_OPCOM_CUR. OPDRV/OPCOM output stage current setting |
| 5:4 | R/W | 0x1 | OPADC1_BIAS_CUR. OPADC1 Bias Current Select |
| 3:2 | R/W | 0x1 | OPADC2_BIAS_CUR. OPADC2 Bias Current Select |
| 1:0 | R/W | 0x1 | OPAAF_BIAS_CUR. OPAAF in ADC Bias Current Select |

4.14.5.137. 0x11 OPMIC、OPVR and OPADC Control(Default Value: 0x55)

| Offset:0x11 | | | Register Name: OPMIC_CTRL |
|-------------|-----|-------------|----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 7:6 | R/W | 0x1 | OPMIC_BIAS_CUR |

| | | | |
|-----|-----|-----|---|
| | | | OPMIC Bias Current Control |
| 5:4 | R/W | 0x1 | OPVR_BIAS_CUR. OPVR Bias Current Control Especially, bit 5 can also control HPCOMFB: =0, HPCOMFB pin can be used to PA when R07_[6:5] is not 11; =1, HPCOMFB pin always can not be used to PA |
| 3:2 | R/W | 0x1 | OPDAC_BIAS_CUR. OPDAC Bias Current Control |
| 1:0 | R/W | 0x1 | OPMIX_BIAS_CUR. OPMIX/OPLPF/OPDRV/OPCOM Bias Current Control |

4.14.5.138. 0x12 ZERO CROSS Control(Default Value: 0x42)

| Offset:0x12 | | | Register Name: ZERO_CROSS_CTRL |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7 | R/W | 0x0 | function enable for master volume change at zero cross over 0: disable; 1: enable |
| 6 | R/W | 0x1 | Timeout control for master volume change at zero cross over 0: 32ms; 1: 64ms |
| 5:4 | R/W | 0x0 | PTDBS HPCOM protect de-bounce time setting 00: 2-3ms; 01: 4-6ms; 10: 8-12ms; 11: 16-24ms at the same time, bit 17 is used to control the AVCCPORFLAG, write 1 to this bit, flag will be clear, and the calibration is done again |
| 3 | R/W | 0x0 | PA_SLOPE_SELECT PA slope select cosine or ramp 0: select cosine 1: select ramp |
| 2:0 | R/W | 0x2 | USB_BIAS_CUR. USB bias current tuning From 23uA to 30uA, Default is 25uA |

4.14.5.139. 0x13 ADC Function Control(Default Value: 0xD6)

| Offset:0x13 | | | Register Name: ADC_FUN_CTRL |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7 | R/W | 0x1 | MMIC BIAS chopper enable 0: disable; 1:enable |
| 6:5 | R/W | 0x2 | MMIC BIAS chopper clock select 00: 250KHz; 01: 500KHz; 10: 1MHz; 11: 2MHz |
| 4 | R/W | 0x1 | DITHER ADC dither on/off control 0: dither off; 1: dither on |
| 3:2 | R/W | 0x1 | DITHER_CLK_SELECT ADC dither clock select 00: ADC FS * (8/9), about 43KHz when FS=48KHz 01: ADC FS * (16/15), about 51KHz when FS=48KHz 10: ADC FS * (4/3), about 64KHz when FS=48KHz 11: ADC FS * (16/9), about 85KHz when FS=48KHz |
| 1:0 | R/W | 0x2 | BIHE_CTRL, BIHE control 00: no BIHE |

| | | | |
|--|--|--|---|
| | | | 01: BIHE=7.5 HOSC 10: BIHE=11.5 HOSC 11: BIHE=15.5 HOSC |
|--|--|--|---|

4.14.5.140. 0x14 Bias & DA16 Calibration Control Register(Default Value: 0x00)

| Offset:0x14 | | | Register Name: CALIBRATION_CTRL |
|-------------|-----|-------------|--|
| bit | R/W | Default/Hex | Description |
| 7 | R/W | 0x0 | PA_SPEED_SELECT PA setup speed control (for testing) 0: slow; 1: fast |
| 6 | R/W | 0x0 | CURRENT_TEST_SELECT Internal current sink test enable (from LINEIN pin) 0:Normal; 1: For Debug |
| 5 | R/W | 0x0 | / |
| 4 | R/W | 0x0 | BIAS and DA16 calibration clock select 0: 1KHz; 1: 500Hz |
| 3 | R/W | 0x0 | BIAS calibration mode select 0: average; 1: single |
| 2 | R/W | 0x0 | BIAS and DA16 calibration control Write 1 to this bit, the calibration will be doing again. Then this bit will be reset to zero automatically |
| 1 | R/W | 0x0 | BIASCALIVERIFY Bias Calibration Verify 0: Calibration; 1: Register setting |
| 0 | R/W | 0x0 | DA16CALIVERIFY DA16 Calibration Verify 0: Calibration; 1: Register setting |

4.14.5.141. 0x15 DA16 Calibration Data(Default Value: 0x80)

| Offset:0x15 | | | Register Name: DA16CALI_DATA |
|-------------|-----|-------------|-------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 7:0 | R | 0x80 | DA16CALI DA16 Calibration Data |

4.14.5.142. 0x17 Bias Calibration Data(Default Value: 0x20)

| Offset:0x17 | | | Register Name: DA16CALI_DATA |
|-------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7:6 | / | / | / |
| 5:0 | R | 0x20 | BIASCALI Bias Calibration Data, 6bit |

4.14.5.143. 0x18 Bias Register Setting Data(Default Value: 0x20)

| Offset:0x18 | | | Register Name: DA16CALI_SET |
|-------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 7:6 | / | / | / |
| 5:0 | R/W | 0x20 | BIASVERIFY Bias Register Setting Data, 6bit |

Sochip

| | | | | |
|-------|-----|-----|--|--|
| | | | 010: TWIO_SDA 100: Reserved 110: PB_EINT7 | 011: Reserved 101: Reserved 111: IO Disable |
| 27 | / | / | / | |
| 26:24 | R/W | 0x7 | PB6_SELECT 000: Input 010: TWIO_SCK 100: Reserved 110: PB_EINT6 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 23 | / | / | / | |
| 22:20 | R/W | 0x7 | PB5_SELECT 000: Input 010: PWM1 100: Reserved 110: PB_EINT5 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 19 | / | / | / | |
| 18:16 | R/W | 0x7 | PB4_SELECT 000: Input 010: PWM0 100: Reserved 110: PB_EINT4 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 15 | / | / | / | |
| 14:12 | R/W | 0x7 | PB3_SELECT 000: Input 010: UART2_CTS 100: Reserved 110: PB_EINT3 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 11 | / | / | / | |
| 10:8 | R/W | 0x7 | PB2_SELECT 000: Input 010: UART2_RTS 100: Reserved 110: PB_EINT2 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 7 | / | / | / | |
| 6:4 | R/W | 0x7 | PB1_SELECT 000: Input 010: UART2_RX 100: Reserved 110: PB_EINT1 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 3 | / | / | / | |
| 2:0 | R/W | 0x7 | PB0_SELECT 000: Input 010: UART2_TX 100: Reserved 110: PB_EINT0 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |

4.15.2.2. PB Configure Register 1 (Default Value: 0x00777777)

| Offset: 0x28 | | | Register Name: PB_CFG1_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:23 | / | / | / |
| 22:20 | R/W | 0x7 | PB13_SELECT |

| | | | | |
|-------|-----|-----|--|--|
| | | | 000: Input 010: JTAG_DI 100: Reserved 110: PB_EINT13 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 19 | / | / | / | |
| | | | PB12_SELECT 000: Input 010: JTAG_DO 100: Reserved 110: PB_EINT12 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 18:16 | R/W | 0x7 | | |
| 15 | / | / | | |
| | | | PB11_SELECT 000: Input 010: JTAG_CK 100: Reserved 110: PB_EINT11 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 14:12 | R/W | 0x7 | | |
| 11 | / | / | | |
| | | | PB10_SELECT 000: Input 010: JTAG_MS 100: Reserved 110: PB_EINT10 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 10:8 | R/W | 0x7 | | |
| 7 | / | / | | |
| | | | PB9_SELECT 000: Input 010: TWI1_SDA 100: Reserved 110: PB_EINT9 | 001: Output 011: UART0_RX 101: Reserved 111: IO Disable |
| 6:4 | R/W | 0x7 | | |
| 3 | / | / | | |
| | | | PB8_SELECT 000: Input 010: TWI1_SCK 100: Reserved 110: PB_EINT8 | 001: Output 011: UART0_TX 101: Reserved 111: IO Disable |
| 2:0 | R/W | 0x7 | | |

4.15.2.3. PB Configure Register 2 (Default Value: 0x00000000)

| Offset: 0x2C | | | Register Name: PB_CFG2_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.4. PB Configure Register 3 (Default Value: 0x00000000)

| Offset: 0x30 | | | Register Name: PB_CFG3_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.5. PB Data Register (Default Value: 0x00000000)

| Offset: 0x34 | | | Register Name: PB_DATA_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| 13:0 | R/W | 0x0 | PB_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read. |

4.15.2.6. PB Multi-Driving Register 0 (Default Value: 0x05555555)

| Offset: 0x38 | | | Register Name: PB_DRV0_REG |
|------------------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| $[2i+1:2i]$ $(i=0\sim13)$ | R/W | 0x1 | PB_DRV PB[n] Multi-Driving Select (n = 0~13) 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |

4.15.2.7. PB Multi-Driving Register 1 (Default Value: 0x00000000)

| Offset: 0x3C | | | Register Name: PB_DRV1_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.8. PB PULL Register 0 (Default Value: 0x00000000)

| Offset: 0x40 | | | Register Name: PB_PULL0_REG |
|------------------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| $[2i+1:2i]$ $(i=0\sim13)$ | R/W | 0x0 | PB_PULL PB[n] Pull-up/down Select (n = 0~13) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved |

4.15.2.9. PB PULL Register 1 (Default Value: 0x00000000)

| Offset: 0x44 | | | Register Name: PB_PULL1_REG |
|--------------|-----|-------------|------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.10. PC Configure Register 0 (Default Value: 0x77777777)

| Offset: 0x48 | | | Register Name: PC_CFG0_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30:28 | R/W | 0x7 | PC7_SELECT 000: Reserved 001: Reserved 010: SDC2_D4 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 27 | / | / | / |
| 26:24 | R/W | 0x7 | PC6_SELECT 000: Input 001: Output 010: SDC2_D3 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 23 | / | / | / |
| 22:20 | R/W | 0x7 | PC5_SELECT 000: Input 001: Output 010: SDC2_D2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 19 | / | / | / |
| 18:16 | R/W | 0x7 | PC4_SELECT 000: Input 001: Output 010: SDC2_D1 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 15 | / | / | / |
| 14:12 | R/W | 0x7 | PC3_SELECT 000: Input 001: Output 010: SDC2_D0 011: SPI0_MOSI 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 11 | / | / | / |
| 10:8 | R/W | 0x7 | PC2_SELECT 000: Input 001: Output 010: SDC2_RST 011: SPI0_CS 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 7 | / | / | / |
| 6:4 | R/W | 0x7 | PC1_SELECT 000: Input 001: Output 010: SDC2_CMD 011: SPI0_CLK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 3 | / | / | / |
| 2:0 | R/W | 0x7 | PC0_SELECT 000: Input 001: Output 010: SDC2_CLK 011: SPI0_MISO 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |

4.15.2.11. PC Configure Register 1 (Default Value: 0x00000777)

| Offset: 0x4C | | | Register Name: PC_CFG1_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:11 | / | / | / |
| 10:8 | R/W | 0x7 | PC10_SELECT 000: Reserved 001: Reserved 010: SDC2_D7 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 7 | / | / | / |
| 6:4 | R/W | 0x7 | PC9_SELECT 000: Reserved 001: Reserved 010: SDC2_D6 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 3 | / | / | / |
| 2:0 | R/W | 0x7 | PC8_SELECT 000: Reserved 001: Reserved 010: SDC2_D5 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |

4.15.2.12. PC Configure Register 2 (Default Value: 0x00000000)

| Offset: 0x50 | | | Register Name: PC_CFG2_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.13. PC Configure Register 3 (Default Value: 0x00000000)

| Offset: 0x54 | | | Register Name: PC_CFG3_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.14. PC Data Register (Default Value: 0x00000000)

| Offset: 0x58 | | | Register Name: PC_DATA_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:11 | / | / | / |
| 10:0 | R/W | 0x0 | PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read. |

4.15.2.15. PC Multi-Driving Register 0 (Default Value: 0x00155555)

| Offset: 0x5C | | | Register Name: PC_DRV0_REG |
|-----------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:22 | / | / | / |
| [2i+1:2i] (i=0~10) | R/W | 0x1 | PC_DRV PC[n] Multi-Driving SELECT (n = 0~10) 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |

4.15.2.16. PC Multi-Driving Register 1 (Default Value: 0x00000000)

| Offset: 0x60 | | | Register Name: PC_DRV1_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.17. PC PULL Register 0 (Default Value: 0x00000000)

| Offset: 0x64 | | | Register Name: PC_PULL0_REG |
|-----------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:22 | / | / | / |
| [2i+1:2i] (i=0~10) | R/W | 0x0 | PC_PULL PC[n] Pull-up/down Select (n = 0~10) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved |

4.15.2.18. PC PULL Register 1 (Default Value: 0x00000000)

| Offset: 0x68 | | | Register Name: PC_PULL1_REG |
|--------------|-----|-------------|------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.19. PD Configure Register 0 (Default Value: 0x77777777)

| Offset: 0x6C | | | Register Name: PD_CFG0_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30:28 | R/W | 0x7 | PD7_SELECT 000:Input 001:Output 010: LCD_D11 011:Reserved 100: RGMII_TXD3/MII_TXD3/RMII_NULL 101:Reserved 110:Reserved 111:IO Disable |
| 27 | / | / | Reserved |
| 26:24 | R/W | 0x7 | PD6_SELECT 000:Input 001:Output 010: LCD_D10 011:Reserved |

| | | | | |
|-------|-----|-----|--|--|
| | | | 100: RGMII_NULL/MII_RXERR/RMII_RXER 110:Reserved 111:IO Disable | 101:Reserved |
| 23 | / | / | / | |
| 22:20 | R/W | 0x7 | PD5_SELECT 000:Input 010: LCD_D7 100: RGMII_RXCTL/MII_RXDV/RMII_NULL 110:Reserved 111:IO Disable | 001:Output 011:Reserved 101:Reserved |
| 19 | / | / | / | |
| 18:16 | R/W | 0x7 | PD4_SELECT 000:Input 010: LCD_D6 100: RGMII_RXCK/MII_RXCK/RMII_NULL 110:Reserved 111:IO Disable | 001:Output 011:Reserved 101:Reserved |
| 15 | / | / | / | |
| 14:12 | R/W | 0x7 | PD3_SELECT 000:Input 010: LCD_D5 100: RGMII_RXD0/MII_RXD0/RMII_RXD0 110:Reserved 111:IO Disable | 001:Output 011:Reserved 101:Reserved |
| 11 | / | / | / | |
| 10:8 | R/W | 0x7 | PD2_SELECT 000:Input 010: LCD_D4 100: RGMII_RXD1/MII_RXD1/RMII_RXD1 110:Reserved 111:IO Disable | 001:Output 011:Reserved 101:Reserved |
| 7 | / | / | / | |
| 6:4 | R/W | 0x7 | PD1_SELECT 000:Input 010: LCD_D3 100: RGMII_RXD2/MII_RXD2/RMII_NULL 110:Reserved 111:IO Disable | 001:Output 011:Reserved 101:Reserved |
| 3 | / | / | / | |
| 2:0 | R/W | 0x7 | PD0_SELECT 000:Input 010: LCD_D2 100: RGMII_RXD3/ MII_RXD3/ RMII_NULL 110:Reserved 111:IO Disable | 001:Output 011:Reserved 101:Reserved |

4.15.2.20. PD Configure Register 1 (Default Value: 0x77777777)

| Offset: 0x70 | | | Register Name: PD_CFG1_REG | |
|--------------|-----|-------------|--|---|
| Bit | R/W | Default/Hex | Description | |
| 31 | / | / | / | |
| 30:28 | R/W | 0x7 | PD15_SELECT 000:Input 010: LCD_D21 100: RGMII_CLKIN/MII_COL/RMII_NULL 110:Reserved 111:IO Disable | 001:Output 011: LVDS_VN1 101:Reserved |
| 27 | / | / | / | |
| 26:24 | R/W | 0x7 | PD14_SELECT 000:Input | 001:Output |

| | | | | | |
|-------|-----|-----|--|---|--------------|
| | | | 010: LCD_D20 100: RGMII_NULL/MII_TXERR/RMII_NULL 110:Reserved | 011: LVDS_VP1 111:IO Disable | 101:Reserved |
| 23 | / | / | / | / | / |
| 22:20 | R/W | 0x7 | PD13_SELECT 000:Input 010: LCD_D19 100: RGMII_TXCTL/MII_TXEN/RMII_TXEN 110:Reserved | 001:Output 011: LVDS_VN0 111:IO Disable | 101:Reserved |
| 19 | / | / | / | / | / |
| 18:16 | R/W | 0x7 | PD12_SELECT 000:Input 010: LCD_D18 100: RGMII_TXCK/MII_TXCK/RMII_TXCK 110:Reserved | 001:Output 011: LVDS_VP0 111:IO Disable | 101:Reserved |
| 15 | / | / | / | / | / |
| 14:12 | R/W | 0x7 | PD11_SELECT 000:Input 010: LCD_D15 100: RGMII_NULL/MII_CRD_V/RMII_CRD_V 110:Reserved | 001:Output 011:Reserved 111:IO Disable | 101:Reserved |
| 11 | / | / | / | / | / |
| 10:8 | R/W | 0x7 | PD10_SELECT 000:Input 010: LCD_D14 100: RGMII_TXD0/MII_TXD0/RMII_TXD0 110:Reserved | 001:Output 011:Reserved 111:IO Disable | 101:Reserved |
| 7 | / | / | / | / | / |
| 6:4 | R/W | 0x7 | PD9_SELECT 000:Input 010: LCD_D13 100: RGMII_TXD1/MII_TXD1/RMII_TXD1 110:Reserved | 001:Output 011:Reserved 111:IO Disable | 101:Reserved |
| 3 | / | / | / | / | / |
| 2:0 | R/W | 0x7 | PD8_SELECT 000:Input 010: LCD_D12 100: RGMII_TXD2/MII_TXD2/RMII_NULL 110:Reserved | 001:Output 011:Reserved 111:IO Disable | 101:Reserved |

4.15.2.21. PD Configure Register 2 (Default Value: 0x00777777)

| Offset: 0x74 | | | Register Name: PD_CFG2_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:23 | / | / | / |
| 22:20 | R/W | 0x7 | PD21_SELECT 000: Input 010: LCD_VSYNC 100: Reserved 110: Reserved |
| 19 | / | / | 001: Output 011: LVDS_VN3 101: Reserved 111: IO Disable |
| 18:16 | R/W | 0x7 | Reserved PD20_SELECT |

| | | | | |
|-------|-----|-----|---|--|
| | | | 000: Input 010: LCD_HSYNC 100: Reserved 110: Reserved | 001: Output 011: LVDS_VP3 101: Reserved 111: IO Disable |
| 15 | / | / | / | |
| | | | PD19_SELECT 000: Input 010: LCD_DE 100: Reserved 110: Reserved | 001: Output 011: LVDS_VNC 101: Reserved 111: IO Disable |
| 14:12 | R/W | 0x7 | | |
| 11 | / | / | / | |
| | | | PD18_SELECT 000: Input 010: LCD_CLK 100: Reserved 110: Reserved | 001: Output 011: LVDS_VPC 101: Reserved 111: IO Disable |
| 10:8 | R/W | 0x7 | | |
| 7 | / | / | / | |
| | | | PD17_SELECT 000: Input 010: LCD_D23 100: MDIO 110: Reserved | 001: Output 011: LVDS_VN2 101: Reserved 111: IO Disable |
| 6:4 | R/W | 0x7 | | |
| 3 | / | / | / | |
| | | | PD16_SELECT 000: Input 010: LCD_D22 100: MDC 110: Reserved | 001: Output 011: LVDS_VP2 101: Reserved 111: IO Disable |
| 2:0 | R/W | 0x7 | | |

4.15.2.22. PD Configure Register 3 (Default Value: 0x00000000)

| Offset: 0x78 | | | Register Name: PD_CFG3_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.23. PD Data Register (Default Value: 0x00000000)

| Offset: 0x7C | | | Register Name: PD_DATA_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:22 | / | / | / |
| 21:0 | R/W | 0x0 | PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read. |

4.15.2.24. PD Multi-Driving Register 0 (Default Value: 0x55555555)

| | |
|--------------|-----------------------------------|
| Offset: 0x80 | Register Name: PD_DRV0_REG |
|--------------|-----------------------------------|

| Bit | R/W | Default/Hex | Description |
|-----------------------|-----|-------------|---|
| [2i+1:2i] (i=0~15) | R/W | 0x1 | PD_DRV PD[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |

4.15.2.25. PD Multi-Driving Register 1 (Default Value: 0x00000555)

| Offset: 0x84 | | | Register Name: PD_DRV1_REG |
|----------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:12 | / | / | / |
| [2i+1:2i] (i=0~5) | R/W | 0x1 | PD_DRV PD[n] Multi-Driving Select (n = 16~21) 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |

4.15.2.26. PD PULL Register 0 (Default Value: 0x00000000)

| Offset: 0x88 | | | Register Name: PD_PULL0_REG |
|-----------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| [2i+1:2i] (i=0~15) | R/W | 0x0 | PD_PULL PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved |

4.15.2.27. PD PULL Register 1 (Default Value: 0x00000000)

| Offset: 0x8C | | | Register Name: PD_PULL1_REG |
|----------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:12 | / | / | Reserved |
| [2i+1:2i] (i=0~5) | R/W | 0x0 | PD_PULL PD[n] Pull-up/down Select (n = 16~21) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved |

4.15.2.28. PE Configure Register 0 (Default Value: 0x77777777)

| Offset: 0x90 | | | Register Name: PE_CFG0_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30:28 | R/W | 0x7 | PE7_SELECT 000: Input 001: Output 010: CSI_D3 011: LCD_D5 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 27 | / | / | / |
| 26:24 | R/W | 0x7 | PE6_SELECT |

| | | | | |
|-------|-----|-----|--|---|
| | | | 000: Input 010: CSI_D2 100: Reserved 110: Reserved | 001: Output 011: LCD_D4 101: Reserved 111: IO Disable |
| 23 | / | / | / | / |
| | | | PE5_SELECT 000: Input 010: CSI_D1 100: Reserved 110: Reserved | 001: Output 011: LCD_D3 101: Reserved 111: IO Disable |
| 22:20 | R/W | 0x7 | | |
| 19 | / | / | / | / |
| | | | PE4_SELECT 000: Input 010: CSI_D0 100: Reserved 110: Reserved | 001: Output 011: LCD_D2 101: Reserved 111: IO Disable |
| 18:16 | R/W | 0x7 | | |
| 15 | / | / | / | / |
| | | | PE3_SELECT 000: Input 010: CSI_VSYNC 100: Reserved 110: Reserved | 001: Output 011: LCD_VSYNC 101: Reserved 111: IO Disable |
| 14:12 | R/W | 0x7 | | |
| 11 | / | / | / | / |
| | | | PE2_SELECT 000: Input 010: CSI_HSYNC 100: Reserved 110: Reserved | 001: Output 011: LCD_HSYNC 101: Reserved 111: IO Disable |
| 10:8 | R/W | 0x7 | | |
| 7 | / | / | / | / |
| | | | PE1_SELECT 000: Input 010: CSI_MCLK 100: Reserved 110: Reserved | 001: Output 011: LCD_DE 101: Reserved 111: IO Disable |
| 6:4 | R/W | 0x7 | | |
| 3 | / | / | / | / |
| | | | PE0_SELECT 000: Input 010: CSI_PCLK 100: Reserved 110: Reserved | 001: Output 011: LCD_CLK 101: Reserved 111: IO Disable |
| 2:0 | R/W | 0x7 | | |

4.15.2.29. PE Configure Register 1 (Default Value: 0x77777777)

| Offset: 0x94 | | | Register Name: PE_CFG1_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| | | | PE15_SELECT 000: Input 010: CSI_D11 100: Reserved 110: Reserved |
| 30:28 | R/W | 0x7 | 001: Output 011: LCD_D15 101: Reserved 111: IO Disable |
| 27 | / | / | / |

| | | | | |
|-------|-----|-----|---|---|
| 26:24 | R/W | 0x7 | PE14_SELECT 000: Input 010: CSI_D10 100: Reserved 110: Reserved | 001: Output 011: LCD_D14 101: Reserved 111: IO Disable |
| 23 | / | / | / | / |
| 22:20 | R/W | 0x7 | PE13_SELECT 000: Input 010: CSI_D9 100: Reserved 110: Reserved | 001: Output 011: LCD_D13 101: Reserved 111: IO Disable |
| 19 | / | / | / | / |
| 18:16 | R/W | 0x7 | PE12_SELECT 000: Input 010: CSI_D8 100: Reserved 110: Reserved | 001: Output 011: LCD_D12 101: Reserved 111: IO Disable |
| 15 | / | / | / | / |
| 14:12 | R/W | 0x7 | PE11_SELECT 000: Input 010: CSI_D7 100: Reserved 110: Reserved | 001: Output 011: LCD_D11 101: Reserved 111: IO Disable |
| 11 | / | / | / | / |
| 10:8 | R/W | 0x7 | PE10_SELECT 000: Input 010: CSI_D6 100: Reserved 110: Reserved | 001: Output 011: LCD_D10 101: Reserved 111: IO Disable |
| 7 | / | / | / | / |
| 6:4 | R/W | 0x7 | PE9_SELECT 000: Input 010: CSI_D5 100: Reserved 110: Reserved | 001: Output 011: LCD_D7 101: Reserved 111: IO Disable |
| 3 | / | / | / | / |
| 2:0 | R/W | 0x7 | PE8_SELECT 000: Input 010: CSI_D4 100: Reserved 110: Reserved | 001: Output 011: LCD_D6 101: Reserved 111: IO Disable |

4.15.2.30. PE Configure Register 2 (Default Value: 0x77777777)

| Offset: 0x98 | | | Register Name: PE_CFG2_REG | |
|--------------|-----|-------------|---|---|
| Bit | R/W | Default/Hex | Description | |
| 31 | / | / | / | |
| 30:28 | R/W | 0x7 | PE23_SELECT 000: Input 010: Reserved 100: UART1_RTS 110: Reserved | 001: Output 011: LCD_D22 101: Reserved 111: IO Disable |

| | | | |
|--|--|---------------|-----------------|
| | | 110: Reserved | 111: IO Disable |
|--|--|---------------|-----------------|

4.15.2.32. PE Data Register (Default Value: 0x00000000)

| Offset: 0xA0 | | | Register Name: PE_DATA_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:25 | / | / | / |
| 24:0 | R/W | 0x0 | PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read. |

4.15.2.33. PE Multi-Driving Register 0 (Default Value: 0x55555555)

| Offset: 0xA4 | | | Register Name: PE_DRV0_REG |
|-----------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| [2i+1:2i] (i=0~15) | R/W | 0x1 | PE_DRV PE[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |

4.15.2.34. PE Multi-Driving Register 1 (Default Value: 0x00015555)

| Offset: 0xA8 | | | Register Name: PE_DRV1_REG |
|----------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:18 | / | / | / |
| [2i+1:2i] (i=0~8) | R/W | 0x1 | PE_DRV PE[n] Multi-Driving Select (n = 16~24) 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |

4.15.2.35. PE PULL Register 0 (Default Value: 0x00000000)

| Offset: 0xAC | | | Register Name: PE_PULL0_REG |
|-----------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| [2i+1:2i] (i=0~15) | R/W | 0x0 | PE_PULL PE[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved |

4.15.2.36. PE PULL Register 1 (Default Value: 0x00000000)

| Offset: 0xB0 | | | Register Name: PE_PULL1_REG |
|--------------|-----|-------------|------------------------------------|
| Bit | R/W | Default/Hex | Description |

| | | | |
|----------------------|-----|-----|--|
| 31:18 | / | / | / |
| [2i+1:2i] (i=0~8) | R/W | 0x0 | PE_PULL PE[n] Pull-up/down Select (n = 16~24) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved |

4.15.2.37. PF Configure Register 0 (Default Value: 0x07373733)

| Offset: 0xB4 | | | Register Name: PF_CFG0_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:27 | / | / | / |
| 26:24 | R/W | 0x7 | PF6_SELECT 000: Input 001: Output 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 23 | / | / | / |
| 22:20 | R/W | 0x3 | PF5_SELECT 000: Input 001: Output 010: SDC0_D2 011: JTAG_CK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 19 | / | / | / |
| 18:16 | R/W | 0x7 | PF4_SELECT 000: Input 001: Output 010: SDC0_D3 011: UART0_RX 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 15 | / | / | / |
| 14:12 | R/W | 0x3 | PF3_SELECT 000: Input 001: Output 010: SDC0_CMD 011: JTAG_DO 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 11 | / | / | / |
| 10:8 | R/W | 0x7 | PF2_SELECT 000: Input 001: Output 010: SDC0_CLK 011: UART0_TX 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 7 | / | / | / |
| 6:4 | R/W | 0x3 | PF1_SELECT 000: Input 001: Output 010: SDC0_D0 011: JTAG_DI 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |
| 3 | / | / | / |
| 2:0 | R/W | 0x3 | PF0_SELECT 000: Input 001: Output 010: SDC0_D1 011: JTAG_MS 100: Reserved 101: Reserved 110: Reserved 111: IO Disable |

4.15.2.38. PF Configure Register 1 (Default Value: 0x00000000)

| Offset: 0xB8 | | | Register Name: PF_CFG1_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.39. PF Configure Register 2(Default Value: 0x00000000)

| Offset: 0xBC | | | Register Name: PF_CFG2_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.40. PF Configure Register 3(Default Value: 0x00000000)

| Offset: 0xC0 | | | Register Name: PF_CFG3_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.41. PF Data Register (Default Value: 0x00000000)

| Offset: 0xC4 | | | Register Name: PF_DATA_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:7 | / | / | / |
| 6:0 | R/W | 0x0 | PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read. |

4.15.2.42. PF Multi-Driving Register 0 (Default Value: 0x00001555)

| Offset: 0xC8 | | | Register Name: PF_DRV0_REG |
|----------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| [2i+1:2i] (i=0~6) | R/W | 0x1 | PF_DRV PF[n] Multi-Driving SELECT (n = 0~6) 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |

4.15.2.43. PF Multi-Driving Register 1 (Default Value: 0x00000000)

| | | | |
|--------------|--|--|-----------------------------------|
| Offset: 0xCC | | | Register Name: PF_DRV1_REG |
|--------------|--|--|-----------------------------------|

| | | | | |
|------|-----|-----|---|--|
| | | | 000: Input 010: SDC1_D1 100: Reserved 110: PG_EINT3 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 11 | / | / | / | |
| | | | PG2_SELECT 000: Input 010: SDC1_D0 100: Reserved 110: PG_EINT2 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 10:8 | R/W | 0x7 | | |
| 7 | / | / | / | |
| | | | PG1_SELECT 000: Input 010: SDC1_CMD 100: Reserved 110: PG_EINT1 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 6:4 | R/W | 0x7 | | |
| 3 | / | / | / | |
| | | | PG0_SELECT 000: Input 010: SDC1_CLK 100: Reserved 110: PG_EINT0 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 2:0 | R/W | 0x7 | | |

4.15.2.47. PG Configure Register 1 (Default Value: 0x00777777)

| Offset: 0xDC | | | Register Name: PG_CFG1_REG | |
|--------------|-----|-------------|---|--|
| Bit | R/W | Default/Hex | Description | |
| 31:23 | / | / | / | |
| | | | PG13_SELECT 000: Input 010: PCM_DIN 100: Reserved 110: PG_EINT13 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 22:20 | R/W | 0x7 | | |
| 19 | / | / | / | |
| | | | PG12_SELECT 000: Input 010: PCM_DOUT 100: Reserved 110: PG_EINT12 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 18:16 | R/W | 0x7 | | |
| 15 | / | / | / | |
| | | | PG11_SELECT 000: Input 010: PCM_BCLK 100: Reserved 110: PG_EINT11 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 14:12 | R/W | 0x7 | | |
| 11 | / | / | / | |
| | | | PG10_SELECT 000: Input 010: PCM_SYNC 100: Reserved 110: PG_EINT10 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 10:8 | R/W | 0x7 | | |
| 7 | / | / | / | |

| | | | | |
|-----|-----|-----|--|--|
| 6:4 | R/W | 0x7 | PG9_SELECT 000: Input 010: UART1_CTS 100: Reserved 110: PG_EINT9 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |
| 3 | / | / | / | |
| 2:0 | R/W | 0x7 | PG8_SELECT 000: Input 010: UART1_RTS 100: Reserved 110: PG_EINT8 | 001: Output 011: Reserved 101: Reserved 111: IO Disable |

4.15.2.48. PG Configure Register 2 (Default Value: 0x00000000)

| Offset: 0xE0 | | | Register Name: PG_CFG2_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.49. PG Configure Register 3 (Default Value: 0x00000000)

| Offset: 0xE4 | | | Register Name: PG_CFG3_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.50. PG Data Register (Default Value: 0x00000000)

| Offset: 0xE8 | | | Register Name: PG_DATA_REG |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| 13:0 | R/W | 0x0 | PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read. |

4.15.2.51. PG Multi-Driving Register 0 (Default Value: 0x05555555)

| Offset: 0xEC | | | Register Name: PG_DRV0_REG |
|-----------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| [2i+1:2i] (i=0~13) | R/W | 0x1 | PG_DRV PG[n] Multi-Driving SELECT (n = 0~13) 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |

4.15.2.52. PG Multi-Driving Register 1 (Default Value: 0x00000000)

| Offset: 0xF0 | | | Register Name: PG_DRV1_REG |
|--------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.53. PG PULL Register 0 (Default Value: 0x00000000)

| Offset: 0xF4 | | | Register Name: PG_PULL0_REG |
|-----------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| [2i+1:2i] (i=0~13) | R/W | 0x0 | PG_PULL PG[n] Pull-up/down Select (n = 0~13) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved |

4.15.2.54. PG PULL Register 1 (Default Value: 0x00000000)

| Offset: 0xF8 | | | Register Name: PG_PULL1_REG |
|--------------|-----|-------------|------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.55. PB External Interrupt Configure Register 0 (Default Value: 0x00000000)

| Offset: 0x220 | | | Register Name: PB_EINT_CFG0_REG |
|----------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| [4i+3:4i] (i=0~7) | R/W | 0 | EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved |

4.15.2.56. PB External Interrupt Configure Register 1 (Default Value: 0x00000000)

| Offset: 0x224 | | | Register Name: PB_EINT_CFG1_REG |
|----------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| [4i+3:4i] (i=0~5) | R/W | 0 | EINT_CFG External INTn Mode (n = 8~13) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level |

| | | | |
|--|--|--|---|
| | | | 0x4: Double Edge (Positive/ Negative) Others: Reserved |
|--|--|--|---|

4.15.2.57. PB External Interrupt Configure Register 2 (Default Value: 0x00000000)

| Offset: 0x228 | | | Register Name: PB_EINT_CFG2_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.58. PB External Interrupt Configure Register 3 (Default Value: 0x00000000)

| Offset: 0x22C | | | Register Name: PB_EINT_CFG3_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.59. PB External Interrupt Control Register (Default Value: 0x00000000)

| Offset: 0x230 | | | Register Name: PB_EINT_CTL_REG |
|-----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| [n] (n=0~13) | R/W | 0 | EINT_CTL External INTn Enable (n = 0~13) 0: Disable 1: Enable |

4.15.2.60. PB External Interrupt Status Register (Default Value: 0x00000000)

| Offset: 0x234 | | | Register Name: PB_EINT_STATUS_REG |
|-----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| [n] (n=0~13) | R/W | 0 | EINT_STATUS External INTn Pending Bit (n = 0~13) 0: No IRQ pending 1: IRQ pending Write '1' to clear it. |

4.15.2.61. PB External Interrupt Debounce Register (Default Value: 0x00000000)

| Offset: 0x238 | | | Register Name: PB_EINT_DEB_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:7 | / | / | / |
| 6:4 | R/W | 0 | DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n. |
| 3:1 | / | / | / |

| | | | |
|---|-----|---|--|
| 0 | R/W | 0 | PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz |
|---|-----|---|--|

4.15.2.62. PG External Interrupt Configure Register 0 (Default Value: 0x00000000)

| Offset: 0x240 | | | Register Name: PG_EINT_CFG0_REG |
|----------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| [4i+3:4i] (i=0~7) | R/W | 0 | EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved |

4.15.2.63. PG External Interrupt Configure Register 1 (Default Value: 0x00000000)

| Offset: 0x244 | | | Register Name: PG_EINT_CFG1_REG |
|----------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| [4i+3:4i] (i=0~5) | R/W | 0 | EINT_CFG External INTn Mode (n = 8~13) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved |

4.15.2.64. PG External Interrupt Configure Register 2 (Default Value: 0x00000000)

| Offset: 0x248 | | | Register Name: PG_EINT_CFG2_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.65. PG External Interrupt Configure Register 3 (Default Value: 0x00000000)

| Offset: 0x24C | | | Register Name: PG_EINT_CFG3_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | / | / | / |

4.15.2.66. PG External Interrupt Control Register (Default Value: 0x00000000)

| Offset: 0x250 | | | Register Name: PG_EINT_CTL_REG |
|-----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| [n] (n=0~13) | R/W | 0 | EINT_CTL External INTn Enable (n = 0~13) 0: Disable 1: Enable |

4.15.2.67. PG External Interrupt Status Register (Default Value: 0x00000000)

| Offset: 0x254 | | | Register Name: PG_EINT_STATUS_REG |
|-----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| [n] (n=0~13) | R/W | 0 | EINT_STATUS External INTn Pending Bit (n = 0~13) 0: No IRQ pending 1: IRQ pending Write '1' to clear it. |

4.15.2.68. PG External Interrupt Debounce Register (Default Value: 0x00000000)

| Offset: 0x258 | | | Register Name: PG_EINT_DEB_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:7 | / | / | / |
| 6:4 | R/W | 0 | DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n. |
| 3:1 | / | / | / |
| 0 | R/W | 0 | PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz |

Chapter 5 Memory

This section describes the S3 external memory from two aspects:

- SDRAM
- SD/MMC

5.1. SDRAM

5.1.1. Overview

One built-in DDR3 memory is in the S3 processor.

Sochip

5.2. SD/MMC

5.2.1. Overview

The SD/MMC controller can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memory), Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card.

The SD/MMC controller includes the following features:

- Supports Secure Digital memory protocol commands (up to SD2.0)
- Supports Secure Digital I/O protocol commands
- Supports Multimedia Card protocol commands (up to eMMC4.41)
- Supports eMMC boot operation and alternative boot operation
- Supports Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Supports one SD (Version 1.0 to 2.0) or MMC (Version 3.3 to eMMC4.41)
- Supports hardware CRC generation and error detection
- Supports programmable baud rate
- Supports host pull-up control
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports SDIO suspend and resume operation
- Supports SDIO read wait
- Supports block size of 1 to 65535 bytes
- Supports descriptor-based internal DMA controller
- Internal 128 bytes FIFO for data transfer

5.2.2. Block Diagram

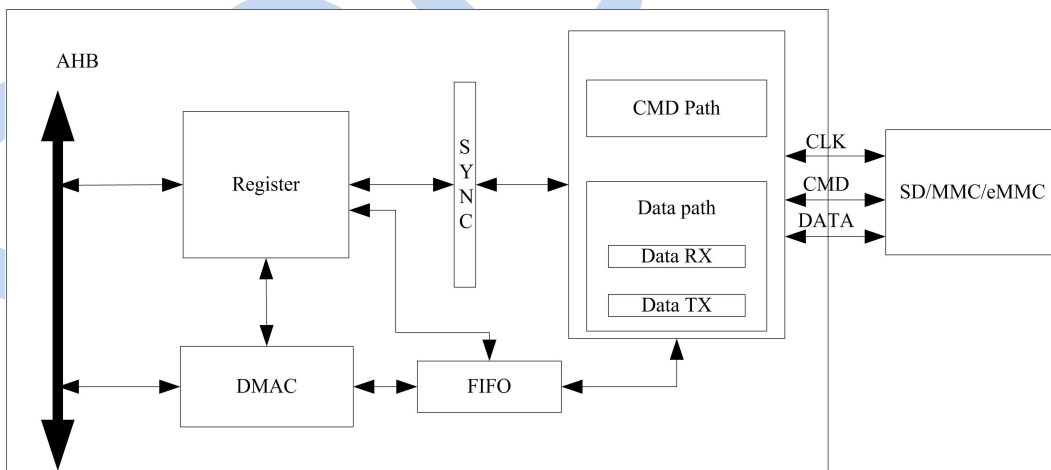


Figure 5-1. SD/MMC Controller Block Diagram

5.2.3. SD/MMC Controller Timing Diagram

Please refer to relative specifications:

- Physical Layer Specification Ver2.00
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)

- JEDEC Standard – JESD84-44, Embedded Multimedia Card (e•MMC) Product Standard

5.2.4. SD/MMC Controller Special Requirement

5.2.4.1. SD/MMC Pin List

| Port Name | Width | Direction | Description |
|-----------|-------|-----------|--------------|
| SDC_CLK | 1 | OUT | Clock output |
| SDC_CMD | 1 | IN/OUT | Command line |
| SDC_DATA | 1/4/8 | IN/OUT | Data line |

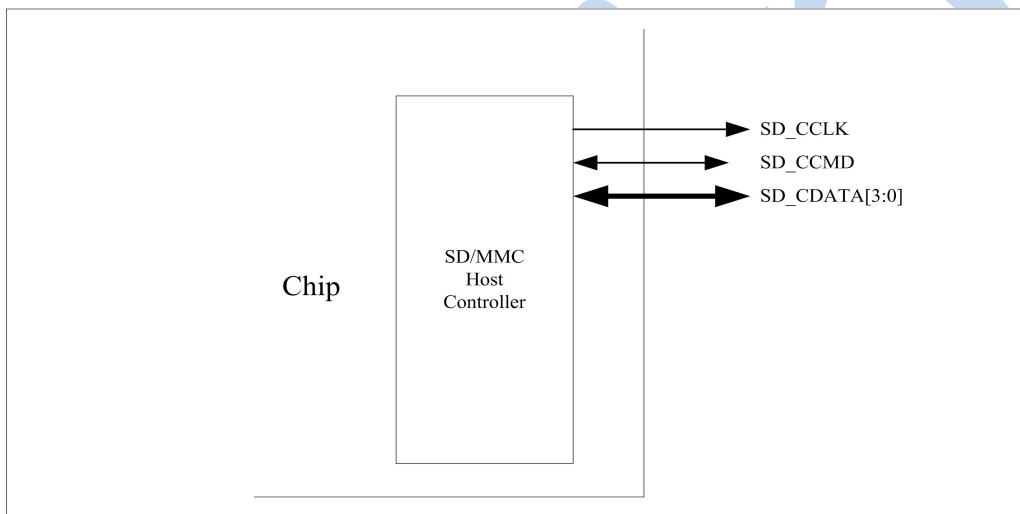


Figure 5-2. SD/MMC Pin Diagram

5.2.5. Internal DMA Controller Description

SD/MMC controller has an internal DMA controller (IDMAC) to transfer data between host memory and SDMMC port. With a descriptor, IDMAC can efficiently move data from source to destination by automatically loading next DMA transfer arguments, which need less CPU intervention. Before transfer data in IDMAC, host driver should construct a descriptor list, configure arguments of every DMA transfer, then launch the descriptor and start the DMA. IDMAC has an interrupt controller, when enabled, it can interrupt the HOST CPU in situations such as data transmission completed or some errors happened.

5.2.5.1. IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

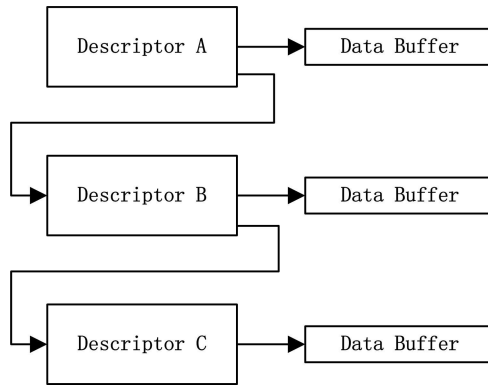


Figure 5-3. SD/MMC IDMAC Descriptor and Buffer

This figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

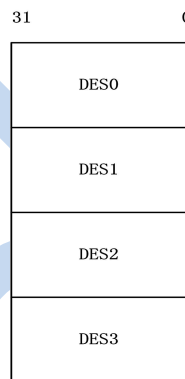


Figure 5-4. Internal Formats of A Descriptor

DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, and DES3 to denote [127:96]bits in a descriptor.

5.2.5.2. DES0 Definition

| Bits | Name | Descriptor |
|------|----------------|---|
| 31 | HOLD | DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over. |
| 30 | ERROR | ERR_FLAG When some error happened in transfer, this bit will be set. |
| 29:5 | / | / |
| 4 | Chain Flag | CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1. |
| 3 | First DES Flag | FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES. |
| 2 | Last DES Flag | LAST_FLAG |

| | | |
|---|---------------------------------|---|
| | | When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer |
| 1 | Disable Interrupt on completion | CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor |
| 0 | / | / |

5.2.5.3. DES1 Definition

| Bits | Name | Descriptor |
|-------|-------------|---|
| 31:13 | / | / |
| 15:0 | Buffer size | BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this field is 0, the DMA ignores this buffer and proceeds to the next descriptor. |

5.2.5.4. DES2 Definition

| Bits | Name | Descriptor |
|------|------------------------|--|
| 31:0 | Buffer address pointer | BUFF_ADDR These bits indicate the physical address of data buffer. The IDMAC ignores DES2[1:0], corresponding to the bus width of 32. |

5.2.5.5. DES3 Definition

| Bits | Name | Descriptor |
|------|-------------------------|--|
| 31:0 | Next descriptor address | NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present. |

5.2.6. SD/MMC Register List

| Module Name | Base Address |
|-------------|--------------|
| SD/MMC0 | 0x01C0F000 |
| SD/MMC1 | 0x01C10000 |
| SD/MMC2 | 0x01C11000 |

| Register Name | Offset | Description |
|---------------|--------|---------------------------|
| SD_GCTL | 0x00 | Control register |
| SD_CKCR | 0x04 | Clock Control register |
| SD_TMOR | 0x08 | Time out register |
| SD_BWDR | 0x0C | Bus Width register |
| SD_BKSR | 0x10 | Block size register |
| SD_BYCR | 0x14 | Byte count register |
| SD_CMDR | 0x18 | Command register |
| SD_CAGR | 0x1c | Command argument register |

| | | |
|--------------|-------|--|
| SD_RESP0 | 0x20 | Response 0 register |
| SD_RESP1 | 0x24 | Response 1 register |
| SD_RESP2 | 0x28 | Response 2 register |
| SD_RESP3 | 0x2C | Response 3 register |
| SD_IMKR | 0x30 | Interrupt mask register |
| SD_MISR | 0x34 | Masked interrupt status register |
| SD_RISR | 0x38 | Raw interrupt status register |
| SD_STAR | 0x3C | Status register |
| SD_FWLR | 0x40 | FIFO Water Level register |
| SD_FUNS | 0x44 | FIFO Function Select register |
| SD_A12A | 0x58 | Auto command 12 argument |
| SD_NTSR | 0x5c | SD NewTiming Set Register |
| SD_SDBG | 0x60 | SD NewTiming Set Debug Register |
| SD_HWRST | 0x78 | Hardware Reset Register |
| SD_DMAC | 0x80 | BUS Mode Control |
| SD_DLBA | 0x84 | Descriptor List Base Address |
| SD_IDST | 0x88 | DMAC Status |
| SD_IDIE | 0x8c | DMAC Interrupt Enable |
| SD_THLDC | 0x100 | Card Threshold Control register |
| SD_DSBD | 0x10c | eMMC4.41 DDR Start Bit Detection Control |
| SD_RES_CRC | 0x110 | CRC status from card/eMMC in write operation |
| SD_DATA7_CRC | 0x114 | CRC Data7 from card/eMMC |
| SD_DATA6_CRC | 0x118 | CRC Data7 from card/eMMC |
| SD_DATA5_CRC | 0x11c | CRC Data7 from card/eMMC |
| SD_DATA4_CRC | 0x120 | CRC Data7 from card/eMMC |
| SD_DATA3_CRC | 0x124 | CRC Data7 from card/eMMC |
| SD_DATA2_CRC | 0x128 | CRC Data7 from card/eMMC |
| SD_DATA1_CRC | 0x12c | CRC Data7 from card/eMMC |
| SD_DATA0_CRC | 0x130 | CRC Data7 from card/eMMC |
| SD_CRC_STA | 0x134 | Response CRC from card/eMMC |
| SD_FIFO | 0x200 | Read/Write FIFO |

5.2.7. SD/MMC Register Description

5.2.7.1. SD Global Control Register(Default Value: 0x0000100)

| Offset: 0x0000 | | | Register Name: SD_CTRL |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | FIFO_AC_MOD FIFO Access Mode 1-AHB bus 0-DMA bus |
| 30:11 | / | / | / |
| 10 | R/W | 0 | DDR_MOD_SEL DDR Mode Select 0 – SDR mode 1 – DDR mode |
| 9 | / | / | reserved |
| 8 | R/W | 1 | CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0 - disable de-bounce |

| | | | |
|-----|-----|---|--|
| | | | 1 – enable de-bounce |
| 7:6 | / | / | / |
| 5 | R/W | 0 | DMA_ENB DMA Global Enable 0 – Disable DMA to transfer data, using AHB bus 1 – Enable DMA to transfer data |
| 4 | R/W | 0 | INT_ENB Global Interrupt Enable 0 – Disable interrupts 1 – Enable interrupts |
| 3 | / | / | / |
| 2 | R/W | 0 | DMA_RST DMA Reset |
| 1 | R/W | 0 | FIFO_RST FIFO Reset 0 – No change 1 – Reset FIFO <i>This bit is auto-cleared after completion of reset operation.</i> |
| 0 | R/W | 0 | SOFT_RST Software Reset 0 – No change 1 – Reset SD/MMC controller <i>This bit is auto-cleared after completion of reset operation.</i> |

5.2.7.2. SD Clock Control Register(Default Value: 0x00000000)

| Offset: 0x0004 | | | Register Name: SD_CLKDIV |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | MASK_DATA0 0 - Do not mask data0 when updata clock ; 1 - Mask data0 when updata clock; Default value : 0; |
| 30:18 | / | / | / |
| 17 | R/W | 0 | CCLK_CTRL Card Clock Output Control 0 – Card clock always on 1 – Turn off card clock when FSM in IDLE state |
| 16 | R/W | 0 | CCLK_ENB Card Clock Enable 0 – Card Clock off 1 – Card Clock on |
| 15:8 | / | / | / |
| 7:0 | R/W | 0 | CCLK_DIV Card clock divider n – Source clock is divided by 2*n.(n=0~255) |

5.2.7.3. SD Timeout Register (Default Value: 0xFFFFF40)

| Offset: 0x0008 | | | Register Name: SD_TMOUT |
|----------------|-----|-------------|--------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:8 | R/W | 0xfffff | DTO_LMT |

| | | | |
|-----|-----|------|-----------------------------------|
| | | | Data Timeout Limit |
| 7:0 | R/W | 0x40 | RTO_LMT Response Timeout Limit |

5.2.7.4. SD Bus Width Register (Default Value: 0x00000000)

| Offset: 0x000c | | | Register Name: SD_CTYPE |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:2 | / | / | / |
| 1:0 | R/W | 0 | CARD_WID Card width 2'b00 – 1-bit width 2'b01 – 4-bit width 2'b1x – 8-bit width |

5.2.7.5. SD Block Size Register (Default Value: 0x00000200)

| Offset: 0x0010 | | | Register Name: SD_BLKSIZE |
|----------------|-----|-------------|----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:16 | / | / | / |
| 15:0 | R/W | 0x200 | BLK_SZ Block size |

5.2.7.6. SD Block Count Register (Default Value: 0x00000200)

| Offset: 0x0014 | | | Register Name: SD_BYTCNT |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x200 | BYTE_CNT Byte counter Number of bytes to be transferred; should be integer multiple of Block Size for block transfers. |

5.2.7.7. SD Command Register (Default Value: 0x00000000)

| Offset: 0x0018 | | | Register Name: SD_CMD |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | CMD_LOAD Start Command. This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit (CMD_OVER) will be set in interrupt register. You should not write any other command before this bit is cleared, or a command busy interrupt bit (CMD_BUSY) will be set in interrupt register. |
| 30 | / | / | / |
| 29 | R/W | 0 | Use Hold Register 0 - CMD and DATA sent to card bypassing HOLD Register 1 - CMD and DATA sent to card through the HOLD Register |

| | | | |
|-------|-----|---|--|
| 28 | R/W | 0 | VOL_SW Voltage Switch 0 – normal command 1 – Voltage switch command, set for CMD11 only |
| 27 | R/W | 0 | BOOT_ABT Boot Abort Setting this bit will terminate the boot operation. |
| 26 | R/W | 0 | EXP_BOOT_ACK Expect Boot Acknowledge. When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card. |
| 25:24 | R/W | 0 | BOOT_MOD Boot Mode 2'b00 – normal command 2'b01 - Mandatory Boot operation 2'b10 - Alternate Boot operation 2'b11 - reserved |
| 23 | / | / | / |
| 22 | / | / | / |
| 21 | R/W | 0 | PRG_CLK Change Clock 0 – Normal command 1 – Change Card Clock; when this bit is set, controller will change clock domain and clock output. No command will be sent. |
| 20:16 | / | / | / |
| 15 | R/W | 0 | SEND_INIT_SEQ Send Initialization 0 – normal command sending 1 – Send initialization sequence before sending this command. |
| 14 | R/W | 0 | STOP_ABT_CMD Stop Abort Command 0 – normal command sending 1 – send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing “I/O Abort” in SDIO CCCR) |
| 13 | R/W | 0 | WAIT_PRE_OVER Wait Data Transfer Over 0 – Send command at once, do not care of data transferring 1 – Wait for data transfer completion before sending current command |
| 12 | R/W | 0 | STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0 – Do not send stop command at end of data transfer 1 – Send stop command automatically at end of data transfer |
| 11 | R/W | 0 | TRANS_MODE Transfer Mode 0 – Block data transfer command 1 – Stream data transfer command |
| 10 | R/W | 0 | TRANS_DIR Transfer Direction 0 – Read operation 1 – Write operation |
| 9 | R/W | 0 | DATA_TRANS Data Transfer 0 – without data transfer 1 – with data transfer |

| | | | |
|-----|-----|---|---|
| 8 | R/W | 0 | CHK_RESP_CRC Check Response CRC 0 – Do not check response CRC 1 – Check response CRC |
| 7 | R/W | 0 | LONG_RESP Response Type 0 –Short Response (48 bits) 1 –Long Response (136 bits) |
| 6 | R/W | 0 | RESP_RCV Response Receive 0 – Command without Response 1 – Command with Response |
| 5:0 | R/W | 0 | CMD_IDX CMD Index Command index value |

5.2.7.8. SD Command Argument Register (Default Value: 0x00000000)

| Offset: 0x001c | | | Register Name: SD_CMDARG |
|----------------|-----|-------------|---------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | CMD_ARG Command argument |

5.2.7.9. SD Response 0 Register (Default Value: 0x00000000)

| Offset: 0x0020 | | | Register Name: SD_RESP0 |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | CMD_RESP0 response 0 Bit[31:0] of response |

5.2.7.10. SD Response 1 Register (Default Value: 0x00000000)

| Offset: 0x0024 | | | Register Name: SD_RESP1 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | CMD_RESP1 response 1 Bit[63:31] of response |

5.2.7.11. SD Response 2 Register (Default Value: 0x00000000)

| Offset: 0x0028 | | | Register Name: SD_RESP2 |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | CMD_RESP2 response 2 Bit[95:64] of response |

5.2.7.12. SD Response 3 Register (Default Value: 0x00000000)

| Offset: 0x002C | | | Register Name: SD_RESP3 |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | CMD_RESP3 response 3 Bit[127:96] of response |

5.2.7.13. SD Interrupt Mask Register (Default Value: 0x00000000)

| Offset: 0x0030 | | | Register Name: SD_INTMASK |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | INT_MASK 0 – interrupt masked 1 – interrupt enabled Bit field defined as following: bit 31 – card removed bit 30 – card inserted bit 17~29 - reserved bit 16 – SDIO interrupt bit 15 – Data End-bit error bit 14 – Auto Stop Command done bit 13 – Data Start Error bit 12 – Command Busy and illegal write bit 11 – FIFO under run/overflow bit 10 – Data starvation timeout /V1.8 Switch Done bit 9 – Data timeout/Boot data start bit 8 – Response timeout/Boot ACK received bit 7 – Data CRC error bit 6 – Response CRC error bit 5 – Data Receive Request bit 4 – Data Transmit Request bit 3 – Data Transfer Complete bit 2 – Command Complete bit 1 – Response Error (no response or response CRC error) bit 0 – Reserved |

5.2.7.14. SD Masked Interrupt Status Register (Default Value: 0x00000000)

| Offset: 0x0034 | | | Register Name: SD_MINTSTS |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | MSKD_ISTA Interrupt status. Enabled only if corresponding bit in mask register is set. Bit field defined as following: bit 31 – card removed bit 30 – card inserted bit 17~29 - reserved bit 16 – SDIO interrupt |

| | | | |
|--|--|--|--|
| | | | bit 15 – Data End-bit error bit 14 – Auto command done bit 13 – Data Start Error bit 12 – Command Busy and illegal write bit 11 – FIFO under run/overflow bit 10 – Data starvation timeout (HTO)/V1.8 Switch Done bit 9 – Data timeout/Boot data start bit 8 – Response timeout/Boot ACK received bit 7 – Data CRC error bit 6 – Response CRC error bit 5 – Data Receive Request bit 4 –Data Transmit Request bit 3 – Data Transfer Complete bit 2 – Command Complete bit 1 – Response Error (no response or response CRC error) bit 0 – Reserved |
|--|--|--|--|

5.2.7.15. SD Raw Interrupt Status Register (Default Value: 0x00000000)

| Offset: 0x0038 | | | Register Name: SD_RINTSTS |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | RAW_ISTA Raw Interrupt Status. <i>This is write-1-to-clear bits.</i> Bit field defined as following: bit 31 – card removed bit 30 – card inserted bit 17~29 - reserved bit 16 – SDIO interrupt bit 15 – Data End-bit error bit 14 – Auto command done bit 13 – Data Start Error bit 12 – Command Busy and illegal write bit 11 – FIFO under run/overflow bit 10 – Data starvation timeout (HTO)/V1.8 Switch Done bit 9 – Data timeout/Boot data start bit 8 – Response timeout/Boot ACK received bit 7 – Data CRC error bit 6 – Response CRC error bit 5 – Data Receive Request bit 4 –Data Transmit Request bit 3 – Data Transfer Complete bit 2 – Command Complete bit 1 – Response Error (no response or response CRC error) bit 0 – Reserved |

5.2.7.16. SD Status Register (Default Value: 0x00000006)

| Offset: 0x003C | | | Register Name: SD_STATUS |
|----------------|-----|-------------|---------------------------------|
| Bit | R/W | Default/Hex | Description |

| | | | |
|-------|---|---|--|
| 31 | R | 0 | DMA_REQ dma_req DMA request signal state |
| 30:22 | / | / | / |
| 21:17 | R | 0 | FIFO_LEVEL FIFO Level Number of filled locations in FIFO |
| 16:11 | R | 0 | RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller |
| 10 | R | 0 | FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy |
| 9 | R | 0 | CARD_BUSY Card data busy Inverted version of DATA[0] 0 – card data not busy 1 – card data busy |
| 8 | R | 0 | CARD_PRESENT Data[3] status level of DATA[3]; checks whether card is present 0 – card not present 1 – card present |
| 7:4 | R | 0 | FSM_STA Command FSM states: 0 – Idle 1 – Send init sequence 2 – Tx cmd start bit 3 – Tx cmd tx bit 4 – Tx cmd index + arg 5 – Tx cmd crc7 6 – Tx cmd end bit 7 – Rx resp start bit 8 – Rx resp IRQ response 9 – Rx resp tx bit 10 – Rx resp cmd idx 11 – Rx resp data 12 – Rx resp crc7 13 – Rx resp end bit 14 – Cmd path wait NCC 15 – Wait; CMD-to-response turnaround |
| 3 | R | 0 | FIFO_FULL FIFO full 1 – FIFO full 0 – FIFO not full |
| 2 | R | 1 | FIFO_EMPTY FIFO Empty 1 - FIFO Empty 0 - FIFO not Empty |
| 1 | R | 1 | FIFO_TX_LEVEL FIFO TX Water Level flag 0 – FIFO didn't reach transmit trigger level 1 - FIFO reached transmit trigger level |
| 0 | R | 0 | FIFO_RX_LEVEL |

| | | | |
|--|--|--|---|
| | | | FIFO TX Water Level flag 0 – FIFO didn't reach receive trigger level 1 - FIFO reached receive trigger level |
|--|--|--|---|

5.2.7.17. SD FIFO Water Level Register (Default Value: 0x000F0000)

| Offset: 0x0040 | | | Register Name: SD_FIFOTH |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30:28 | R/W | 0 | <p>BSIZE_OF_TRANS Burst size of multiple transaction 000 – 1 transfers 001 – 4 010 – 8 011 – 16 100 – 32 101 – 64 110 – 128 111 – 256</p> <p>Should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD. A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) Recommended: MSize = 8, TX_TL = 16, RX_TL = 15</p> |
| 27:21 | R | 0 | / |
| 20:16 | R/W | 0xF | <p>RX_TL Rx Trigger Level 0x0~0x1e – RX Trigger Level is 0~30 0x1f – reserved</p> <p>FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 15 (means greater than 15)</p> |
| 15:5 | R | 0 | / |
| 4:0 | R/W | 0 | <p>TX_TL TX Trigger Level 0x1~0xf – TX Trigger Level is 1~31 0x0 – no trigger</p> <p>FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 16 (means less than or equal to 16)</p> |

5.2.7.18. SD Function Select Register (Default Value: 0x00000000)

| | |
|----------------|-------------------------------|
| Offset: 0x0044 | Register Name: SD_CTRL |
|----------------|-------------------------------|

| Bit | R/W | Default/Hex | Description |
|-------|-----|-------------|---|
| 31:16 | R/W | 0 | CEATA_EN CEATA Support ON/OFF 0xcea – CEATA support on. All hidden CEATA relative bits are accessible normally and these 16 bits return value of 0x1 when be read. Other value – CEATA support off. All hidden CEATA relative bits cannot be access and these 16 bits return value of 0 when be read. |
| 15:3 | / | / | / |
| 2 | R/W | 0 | ABT_RDATA Abort Read Data 0 – Ignored 1 –After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. <i>This bit is auto-cleared once controller reset to idle state.</i> |
| 1 | R/W | 0 | READ_WAIT Read Wait 0 – Clear SDIO read wait 1 – Assert SDIO read wait |
| 0 | R/W | 0 | HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0 – Ignored 1 – Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. <i>This bit is auto-cleared after response is sent.</i> |

5.2.7.19. SD Auto Command 12 Register (Default Value: 0x0000ffff)

| Offset: 0x0058 | | | Register Name: SD_A12A |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | / | / | / |
| 0:15 | R/W | 0xffff | SD_A12A. SD_A12A set the argument of command 12 automatically send by controller |

5.2.7.20. SD NewTiming Set Register (Default Value: 0x00000001,only used in SDC2)

| Offset: 0x005C | | | Register Name: SD_NTZR_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | MODE_SELEC 0 - Old mode of Sample/Output Timing ; 1 - New mode of Sample/Output Timing; Default value : 0; |
| 30:6 | R/W | 0x00 | SAMPLE_TIMING_PHASE(RX) 00 - Sample timing phase offset 90。 ; 01 - Sample timing phase offset 180。 ; 10 - Sample timing phase offset 270。 ; 11 - Ignore; Default value : 00; |

| | | | |
|-----|-----|------|---|
| 3:2 | / | / | / |
| 1:0 | R/W | 0x01 | OUTPUT_TIMING_PHASE(TX) 00 - Output timing phase offset 90° ; 01 - Output timing phase offset 180° ; 10 - Output timing phase offset 270° ; 11 - Ignore; Default value : 01; |

5.2.7.21. SD Hardware Reset Register (Default Value: 0x00000001)

| Offset: 0x0078 | | | Register Name: SD_HWRST |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 1 | HW_RESET. 1 – Active mode 0 – Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized. |

5.2.7.22. SD DMAC Control Register (Default Value: 0x00000000)

| Offset: 0x0080 | | | Register Name: SD_BUS_MODE |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | W | 0 | DES_LOAD_CTRL When DMAC fetches a descriptor, if the valid bit of a descriptor is not set, DMAC FSM will go to the suspend state. Setting this bit will make DMAC re-fetch descriptor again and do the transfer normally. |
| 30:11 | / | / | / |
| 10:8 | R | 0 | PRG_BURST_LEN Programmable Burst Length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of FIFOTH register. In order to change this value, write the required value to FIFOTH register. This is an encode value as follows. 000 – 1 transfers 001 – 4 transfers 010 – 8 transfers 011 – 16 transfers 100 – 32 transfers 101 – 64 transfers 110 – 128 transfers 111 – 256 transfers Transfer unit is either 16, 32, or 64 bits, based on HDATA_WIDTH. PBL is a read-only value. |
| 7 | R/W | 0 | IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write. |
| 6:2 | R/W | 0 | DES_SKIP_LEN Descriptor Skip Length. |

| | | | |
|---|-----|---|---|
| | | | Specifies the number of Word to skip between two unchained descriptors. This is applicable only for dual buffer structure. Default value is set to 4 DWORD. |
| 1 | R/W | 0 | FIX_BUST_CTRL Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations. |
| 0 | R/W | 0 | IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle. |

5.2.7.23. SD Descriptor List Base Address Register (Default Value: 0x00000000)

| Offset: 0x0084 | | | Register Name: SD_DLBA |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | DES_BASE_ADDR Start of Descriptor List. Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only. |

5.2.7.24. SD DMAC Status Register (Default Value: 0x0000_0000)

| Offset: 0x0088 | | | Register Name: SD_DSR |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:17 | / | / | / |
| 16:13 | R | 0 | DMAC_FSM_STA DMAC FSM present state. 0 – DMA_IDLE 1 – DMA_SUSPEND 2 – DESC_RD 3 – DESC_CHK 4 – DMA_RD_REQ_WAIT 5 – DMA_WR_REQ_WAIT 6 – DMA_RD 7 – DMA_WR 8 – DESC_CLOSE This bit is read-only. |
| 12:10 | R | 0 | DMAC_ERR_STA Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDSTS[2]) set. This field does not generate an interrupt. 3'b001 – Host Abort received during transmission 3'b010 – Host Abort received during reception Others: Reserved EB is read-only. |
| 9 | R/W | 0 | ABN_INT_SUM Abnormal Interrupt Summary. Logical OR of the following: |

| | | | |
|-----|-----|---|---|
| | | | <p>IDSTS[2] – Fatal Bus Interrupt IDSTS[4] – DU bit Interrupt IDSTS[5] – Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.</p> |
| 8 | R/W | 0 | <p>NOR_INT_SUM Normal Interrupt Summary. Logical OR of the following: IDSTS[0] – Transmit Interrupt IDSTS[1] – Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.</p> |
| 7:6 | / | / | / |
| 5 | R/W | 0 | <p>ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE – End Bit Error RTO – Response Timeout/Boot Ack Timeout RCRC – Response CRC SBE – Start Bit Error DRTO – Data Read Timeout/BDS timeout DCRC – Data CRC for Receive RE – Response Error <i>Writing 1 clears this bit.</i></p> |
| 4 | R/W | 0 | <p>DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DESO[31]=0). Writing a 1 clears this bit.</p> |
| 3 | / | / | / |
| 2 | R/W | 0 | <p>FATAL_BERR_INT Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.</p> |
| 1 | R/W | 0 | <p>RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.</p> |
| 0 | R/W | 0 | <p>TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a '1' clears this bit.</p> |

5.2.7.25. SD DMAC Interrupt Enable Register (Default Value: 0x00000000)

| Offset: 0x008C | | | Register Name: SD_IDIE_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:10 | / | / | / |
| 9 | R/W | 0 | <p>ABN_INT_ENB Abnormal Interrupt Summary Enable. When set, an abnormal interrupt is enabled. This bit enables the following</p> |

| | | | |
|-----|-----|---|---|
| | | | bits: IDINTEN[2] – Fatal Bus Error Interrupt IDINTEN[4] – DU Interrupt IDINTEN[5] – Card Error Summary Interrupt |
| 8 | R/W | 0 | NOR_INT_ENB Normal Interrupt Summary Enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: IDINTEN[0] – Transmit Interrupt IDINTEN[1] – Receive Interrupt |
| 7:6 | / | / | / |
| 5 | R/W | 0 | ERR_SUM_INT_ENB Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary. |
| 4 | R/W | 0 | DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the DU interrupt is enabled. |
| 3 | / | / | / |
| 2 | R/W | 0 | FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled. |
| 1 | R/W | 0 | RX_INT_ENB Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled. |
| 0 | R/W | 0 | TX_INT_ENB Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled. |

5.2.7.26. Card Threshold Control Register (Default Value: 0x00000000)

| Offset: 0x0100 | | | Register Name: SD_THLD_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| 27:16 | R/W | 0 | CARD_RD_THLD Card Read Threshold Size |
| 15:1 | / | / | / |
| 0 | R/W | 0 | CARD_RD_THLD_ENB Card Read Threshold Enable 0 – Card Read Threshold Disable 1 - Card Read Threshold Enable Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO |

5.2.7.27. eMMC4.41 DDR Start Bit Detection Control Register (Default Value: 0x00000000)

| | |
|----------------|---|
| Offset: 0x010C | Register Name: EMMC_DDR_SBIT_DET_REG |
|----------------|---|

| Bit | R/W | Default/Hex | Description |
|------|-----|-------------|---|
| 31:1 | / | / | / |
| 0 | R/W | 0 | <p>HALF_START_BIT</p> <p>Control for start bit detection mechanism inside mstorage based on duration of start bit.</p> <p>For eMMC 4.41, start bit can be:</p> <p>0 - Full cycle</p> <p>1 - Less than one full cycle</p> <p>Set HALF_START_BIT=1 for eMMC 4.41 and above; set to 0 for SD applications.</p> |

5.2.7.28. SD Response CRC Register (Default Value: 0x00000000)

| Offset: 0x0110 | | | Register Name: RESP_CRC_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:7 | / | / | / |
| 6:0 | R | 0 | <p>RESP_CRC</p> <p>Response CRC</p> <p>Response CRC from card/eMMC.</p> |

5.2.7.29. SD Data7 CRC Register (Default Value: 0x00000000)

| Offset: 0x0114 | | | Register Name: DATA7_CRC_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | <p>DATA7_CRC</p> <p>Data[7] CRC</p> <p>CRC in data[7] from card/eMMC. In DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In SDR mode, the higher of 16 bits indicate the CRC of all data.</p> |

5.2.7.30. SD Data6 CRC Register (Default Value: 0x00000000)

| Offset: 0x0118 | | | Register Name: DATA6_CRC_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | <p>DATA6_CRC</p> <p>Data[6] CRC</p> <p>CRC in data[6] from card/eMMC. In DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In SDR mode, the higher of 16 bits indicate the CRC of all data.</p> |

5.2.7.31. SD Data5 CRC Register (Default Value: 0x00000000)

| Offset: 0x011c | | | Register Name: DATA5_CRC_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | <p>DATA5_CRC</p> <p>Data[5] CRC</p> <p>CRC in data[5] from card/eMMC. In DDR mode, the higher 16 bits indicate the</p> |

| | | | |
|--|--|--|--|
| | | | CRC of even data,and the lower 16bits indicate the CRC of odd data.In SDR mode,the higher of 16 bits indicate the CRC of all data. |
|--|--|--|--|

5.2.7.32. SD Data4 CRC Register (Default Value: 0x00000000)

| Offset: 0x0120 | | | Register Name: DATA4_CRC_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | DATA4_CRC Data[4] CRC CRC in data[4] from card/eMMC.In DDR mode,the higher 16 bits indicate the CRC of even data,and the lower 16bits indicate the CRC of odd data.In SDR mode,the higher of 16 bits indicate the CRC of all data. |

5.2.7.33. SD Data3 CRC Register (Default Value: 0x00000000)

| Offset: 0x0124 | | | Register Name: DATA3_CRC_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | DATA3_CRC Data[3] CRC CRC in data[3] from card/eMMC.In DDR mode,the higher 16 bits indicate the CRC of even data,and the lower 16bits indicate the CRC of odd data.In SDR mode,the higher of 16 bits indicate the CRC of all data. |

5.2.7.34. SD Data2 CRC Register (Default Value: 0x00000000)

| Offset: 0x0128 | | | Register Name: DATA2_CRC_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | DATA2_CRC Data[2] CRC CRC in data[2] from card/eMMC.In DDR mode,the higher 16 bits indicate the CRC of even data,and the lower 16bits indicate the CRC of odd data.In SDR mode,the higher of 16 bits indicate the CRC of all data. |

5.2.7.35. SD Data1 CRC Register (Default Value: 0x00000000)

| Offset: 0x012c | | | Register Name: DATA1_CRC_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | DATA1_CRC Data[1] CRC CRC in data[1] from card/eMMC.In DDR mode,the higher 16 bits indicate the CRC of even data,and the lower 16bits indicate the CRC of odd data.In SDR mode,the higher of 16 bits indicate the CRC of all data. |

5.2.7.36. SD Data0 CRC Register (Default Value: 0x00000000)

| | | | |
|----------------|--|--|-------------------------------------|
| Offset: 0x0130 | | | Register Name: DATA0_CRC_REG |
|----------------|--|--|-------------------------------------|

| Bit | R/W | Default/Hex | Description |
|------|-----|-------------|--|
| 31:0 | R | 0 | DATA0_CRC Data[0] CRC CRC in data[0] from card/eMMC. In DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In SDR mode, the higher of 16 bits indicate the CRC of all data. |

5.2.7.37. SD CRC Status Register (Default Value: 0x00000000)

| Offset: 0x0134 | | | Register Name: CRC_STA_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:3 | / | / | / |
| 2:0 | R | 0 | CRC_STA CRC Status CRC status from card/eMMC in write operation Positive CRC status token: 3'b010 Negative CRC status token: 3'b101 |

5.2.7.38. SD FIFO Register (Default Value: 0x00000000)

| Offset: 0x0200 | | | Register Name: SD_FIFO_REG |
|----------------|-----|-------------|-----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | TX/RX_FIFO Data FIFO |

Chapter 6 Image

This section describes the image of S3:

- CSI
- MIPI CSI2

6.1. CSI

6.1.1. Overview

The CSI includes the following features:

CSI

- Support 8/10/12-bit yuv422 CMOS sensor interface
- Support 8-bit BT656 interface ,support CCIR656 protocol for NTSC and PAL
- Support ITU-R BT1120 protocol for HD-CIF system
- Support 16bit interface with separate syncs
- Support parralel interface still capture resolution up to 5M,video capture resolution up to 1080p@30fps
- Support MIPI interface still capture resolution up to 8M,video capture resolution up to 1080p@60fps
- Support PIP(picture in picture)

CCI

- Compatible with i2c transmission in 7 bit slave ID + 1 bit R/W
- Automatic transmission
- 0/8/16/32-bit register address supported
- 8/16/32-bit data supported
- 64bytes-FIFO input CCI data supported
- Synchronized with CSI signal and delay trigger supported
- Repeated transmission with sync signal supported

6.1.2. Functionalities Description

6.1.2.1. Block Diagram

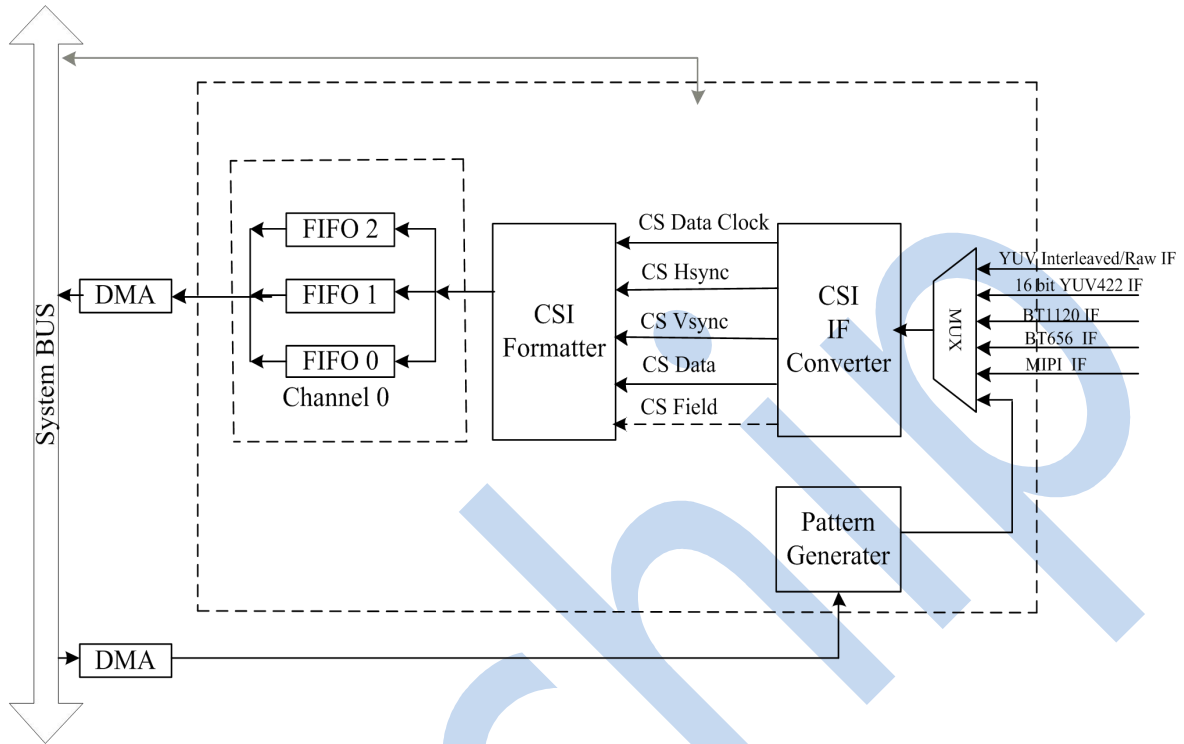


Figure 6-1. CSI Block Diagram

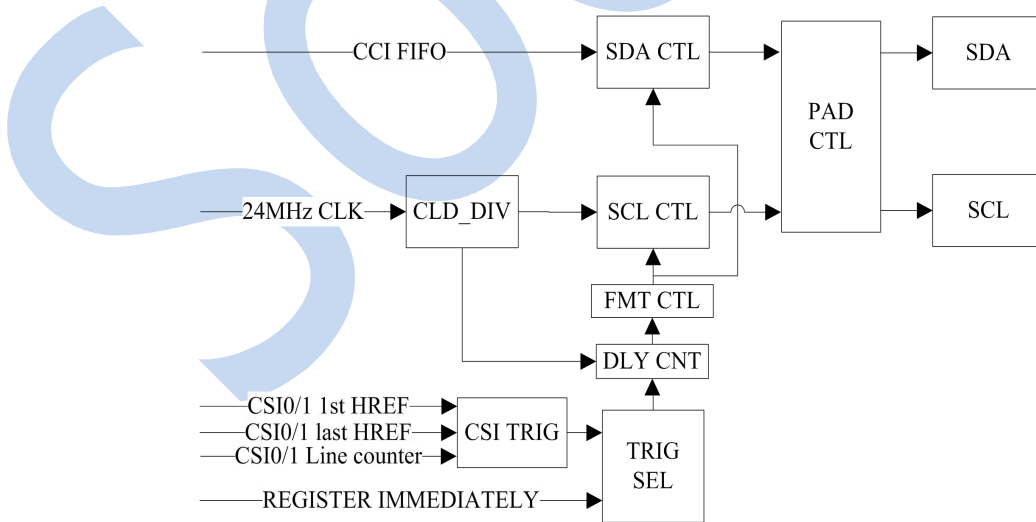


Figure 6-2. CCI Block Diagram

6.1.2.2. CSI FIFO Distribution

| Interface | YUYV422 Interleaved/RAW | BT656 /BT1120 Interface | MIPI Interface |
|-----------|-------------------------|-------------------------|----------------|
|-----------|-------------------------|-------------------------|----------------|

| Input format | YUV422 | | Raw | YUV422 | | YUV422/YUV420 | | Raw |
|---------------|-------------------|--------------------------|-----------------|--------|-----------------|---------------|-----------------|-----------------------|
| Output format | Planar | UV combined/ MB | Raw/RGB /PRGB | Planar | UV combined/ MB | Planar | UV combined/ MB | Pass-Through /Padding |
| CH0_FIFO0 | Y pixel data | Y pixel data | All pixels data | Y | Y | Y | Y | All pixels data |
| CH0_FIFO1 | Cb (U) pixel data | Cb (U) Cr (V) pixel data | - | Cb (U) | CbCr (UV) | Cb (U) | CbCr (UV) | - |
| CH0_FIFO2 | Cr (V) pixel data | - | - | Cr (V) | - | Cr (V) | - | - |

6.1.2.3. Pin Mapping

| pin | 8bit | 10bit | 12bit | 16bit |
|-----|------|-------|-------|-------|
| P0 | - | - | D0 | Y0 |
| P1 | - | - | D1 | Y1 |
| P2 | - | D0 | D2 | Y2 |
| P3 | - | D1 | D3 | Y3 |
| P4 | D0 | D2 | D4 | Y4 |
| P5 | D1 | D3 | D5 | Y5 |
| P6 | D2 | D4 | D6 | Y6 |
| P7 | D3 | D5 | D7 | Y7 |
| P8 | D4 | D6 | D8 | C0 |
| P9 | D5 | D7 | D9 | C1 |
| P10 | D6 | D8 | D10 | C2 |
| P11 | D7 | D9 | D11 | C3 |
| P12 | - | - | - | C4 |
| P13 | - | - | - | C5 |
| P14 | - | - | - | C6 |
| P15 | - | - | - | C7 |

6.1.2.4. Timing

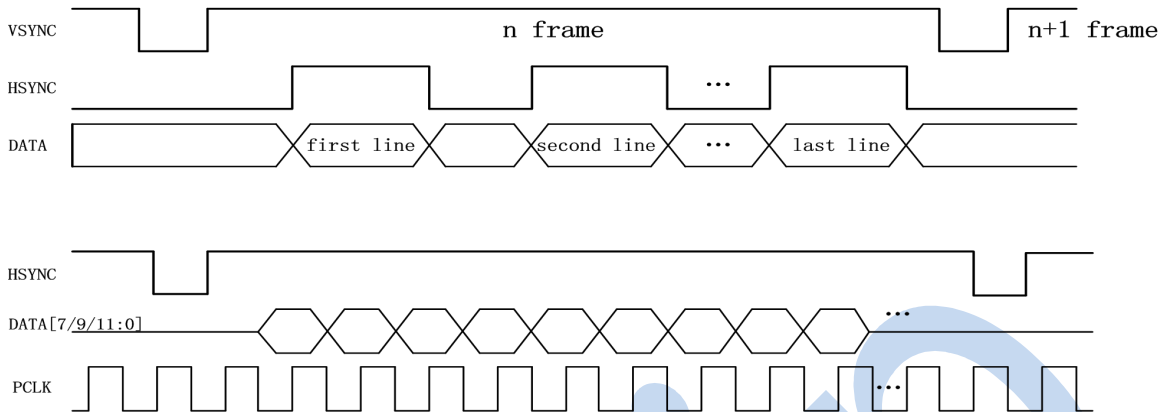


Figure 6-3. 8/10/12-bit CMOS Sensor Interface Timing
(clock rising edge sample.vsync valid = positive,hsync valid = positive)

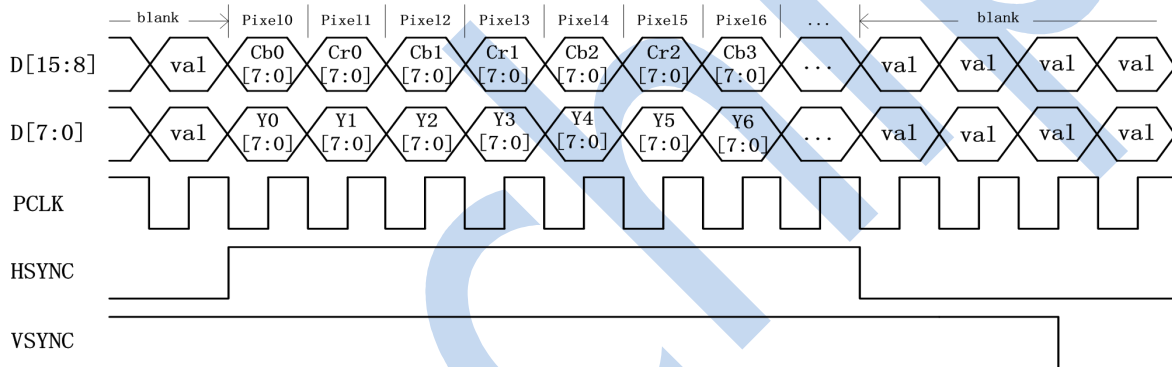


Figure 6-4. 16-bit YCbCr4:2:2 with separate syncs Timing
(clock rising edge sample.vsync valid = positive,hsync valid = positive)

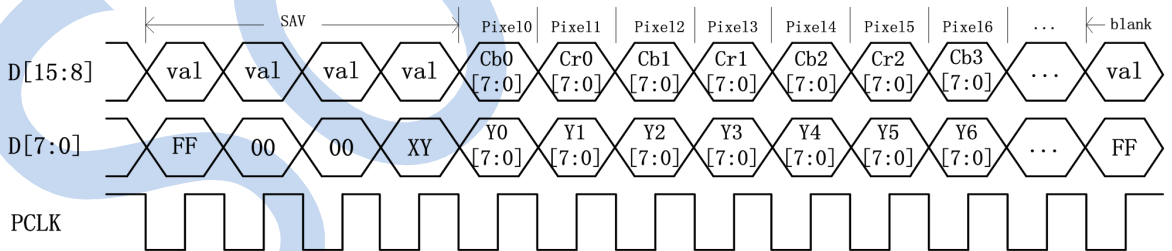


Figure 6-5. 16-bit YCbCr4:2:2 with embedded syncs(BT1120) Timing

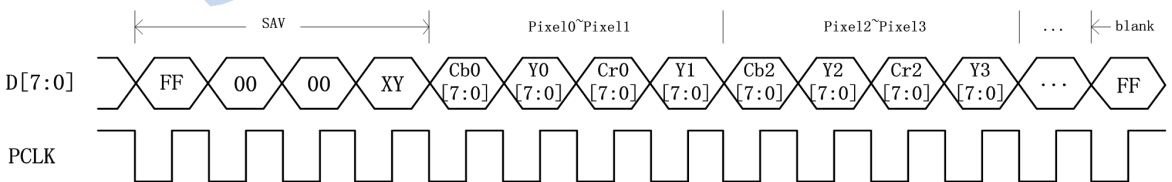


Figure 6-6. 8-bit YCbCr4:2:2 with embedded syncs(BT656) Timing

6.1.2.5. Bit Definition

CCIR656 Header Data Bit Definition:

| Data Bit | First Word(0xFF) | Second Word(0x00) | Third Word(0x00) | Fourth Word |
|---------------|------------------|-------------------|------------------|-------------|
| CS D[9] (MSB) | 1 | 0 | 0 | 1 |
| CS D[8] | 1 | 0 | 0 | F |
| CS D[7] | 1 | 0 | 0 | V |
| CS D[6] | 1 | 0 | 0 | H |
| CS D[5] | 1 | 0 | 0 | P3 |
| CS D[4] | 1 | 0 | 0 | P2 |
| CS D[3] | 1 | 0 | 0 | P1 |
| CS D[2] | 1 | 0 | 0 | P0 |
| CS D[1] | x | x | x | x |
| CS D[0] | x | x | x | x |

Note:

For compatibility with 8-bit interface, CS D[1] and CS D[0] are not defined.

| Decode | F | V | H | P3 | P2 | P1 | P0 |
|-------------------------------------|---|---|---|----|----|----|----|
| Field 1 start of active video (SAV) | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Field 1 end of active video (EAV) | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| Field 1 SAV (digital blanking) | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| Field 1 EAV (digital blanking) | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| Field 2 SAV | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| Field 2 EAV | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| Field 2 SAV (digital blanking) | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Field 2 EAV (digital blanking) | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

Multi-Channel:

| Condition | | | 656FVH Value | | | SAV-EAV Code | | | | | | |
|-----------|--------|--------|--------------|---|---|--------------|--------|-------|--------|------|------|------|
| Field | V-time | H-time | F | V | H | First | Second | Third | Fourth | | | |
| | | | | | | | | | Ch1 | Ch2 | Ch3 | Ch4 |
| EVEN | BLANK | EAV | 1 | 1 | 1 | 0xFF | 0x00 | 0x00 | 0xF0 | 0xF1 | 0xF2 | 0xF3 |
| EVEN | BLANK | SAV | 1 | 1 | 0 | 0xFF | 0x00 | 0x00 | 0xE0 | 0xE1 | 0xE2 | 0xE3 |
| EVEN | BLANK | EAV | 1 | 0 | 1 | 0xFF | 0x00 | 0x00 | 0xD0 | 0xD1 | 0xD2 | 0xD3 |
| EVEN | BLANK | SAV | 1 | 0 | 0 | 0xFF | 0x00 | 0x00 | 0xC0 | 0xC1 | 0xC2 | 0xC3 |
| ODD | BLANK | EAV | 0 | 1 | 1 | 0xFF | 0x00 | 0x00 | 0xB0 | 0xB1 | 0xB2 | 0xB3 |
| ODD | BLANK | SAV | 0 | 1 | 0 | 0xFF | 0x00 | 0x00 | 0xA0 | 0xA1 | 0xA2 | 0xA3 |
| ODD | ACTIVE | EAV | 0 | 0 | 1 | 0xFF | 0x00 | 0x00 | 0x90 | 0x91 | 0x92 | 0x93 |
| ODD | ACTIVE | SAV | 0 | 0 | 0 | 0xFF | 0x00 | 0x00 | 0x80 | 0x81 | 0x82 | 0x83 |

6.1.3. CSI Register list

| Module Name | Base Address |
|-------------|--------------|
|-------------|--------------|

| | |
|------|------------|
| CSI0 | 0x01CB0000 |
| CSI1 | 0x01CB4000 |

| Register Name | Offset | Register name |
|-----------------------------|--------|---|
| CSI_EN_REG | 0x0000 | CSI Enable register |
| CSI_IF_CFG_REG | 0x0004 | CSI Interface Configuration Register |
| CSI_CAP_REG | 0x0008 | CSI Capture Register |
| CSI_SYNC_CNT_REG | 0x000C | CSI Synchronization Counter Register |
| CSI_FIFO_THRS_REG | 0x0010 | CSI FIFO Threshold Register |
| CSI_BT656_HEAD_CFG_REG | 0x0014 | CSI BT656 Header Configuration Register |
| CSI_PTN_LEN_REG | 0x0030 | CSI Pattern Generation Length register |
| CSI_PTN_ADDR_REG | 0x0034 | CSI Pattern Generation Address register |
| CSI_VER_REG | 0x003C | CSI Version Register |
| CSI_C0_CFG_REG | 0x0044 | CSI Channel_0 configuration register |
| CSI_C0_SCALE_REG | 0x004C | CSI Channel_0 scale register |
| CSI_C0_F0_BUFA_REG | 0x0050 | CSI Channel_0 FIFO 0 output buffer-A address register |
| CSI_C0_F1_BUFA_REG | 0x0058 | CSI Channel_0 FIFO 1 output buffer-A address register |
| CSI_C0_F2_BUFA_REG | 0x0060 | CSI Channel_0 FIFO 2 output buffer-A address register |
| CSI_C0_CAP_STA_REG | 0x006C | CSI Channel_0 status register |
| CSI_C0_INT_EN_REG | 0x0070 | CSI Channel_0 interrupt enable register |
| CSI_C0_INT_STA_REG | 0x0074 | CSI Channel_0 interrupt status register |
| CSI_C0_FLD1_VSIZE_REG | 0x0078 | CSI Channel_0 filed1 vertical size register |
| CSI_C0_HSIZE_REG | 0x0080 | CSI Channel_0 horizontal size register |
| CSI_C0_VSIZE_REG | 0x0084 | CSI Channel_0 vertical size register |
| CSI_C0_BUF_LEN_REG | 0x0088 | CSI Channel_0 line buffer length register |
| CSI_C0_FLIP_SIZE_REG | 0x008C | CSI Channel_0 flip size register |
| CSI_C0_FRM_CLK_CNT_REG | 0x0090 | CSI Channel_0 frame clock counter register |
| CSI_C0_ACC_ITNL_CLK_CNT_REG | 0x0094 | CSI Channel_0 accumulated and internal clock counter register |
| CSI_C0_FIFO_STAT_REG | 0x0098 | CSI Channel_0 FIFO Statistic Register |
| CSI_C0_PCLK_STAT_REG | 0x009C | CSI Channel_0 PCLK Statistic Register |
| CCI_CTRL | 0x3000 | CCI control register |
| CCI_CFG | 0x3004 | CCI transmission config register |
| CCI_FMT | 0x3008 | CCI packet format register |
| CCI_BUS_CTRL | 0x300C | CCI bus control register |
| CCI_INT_CTRL | 0x3014 | CCI interrupt control register |
| CCI_LC_TRIG | 0x3018 | CCI line counter trigger register |
| CCI_FIFO_ACC | 0x3100 | CCI FIFO access register |

6.1.4. CSI Register Description

6.1.4.1. CSI Enable Register (Default Value: 0x00000000)

| | |
|----------------|-----------------------------------|
| Offset: 0x0000 | Register Name: CSI0_EN_REG |
|----------------|-----------------------------------|

| Bit | R/W | Default/Hex | Description |
|-------|-----|-------------|---|
| 31 | / | / | / |
| 30 | R/W | 0x0 | VER_EN CSI Version Register Read Enable: 0: Disable 1: Enable |
| 29:24 | / | / | / |
| 23:16 | R/W | 0x0 | PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1. |
| 15:9 | / | / | / |
| 8 | R/W | 0x0 | SRAM_PWDN 0: SRAM in normal 1: SRAM in power down |
| 7:5 | / | / | / |
| 4 | R/W | 0x0 | PTN_START CSI Pattern Generating Start 0: Finish other: Start Software write this bit to "1" to start pattern generating from DRAM. When finished, the hardware will clear this bit to "0" automatically. Generating cycles depends on PTN_CYCLE. |
| 3 | R/W | 0x0 | CLK_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync |
| 2 | R/W | 0x0 | CLK_CNT_EN clk count per frame enable |
| 1 | R/W | 0x0 | PTN_GEN_EN Pattern Generation Enable |
| 0 | R/W | 0x0 | CSI_EN Enable 0: Reset and disable the CSI module 1: Enable the CSI module |

6.1.4.2. CSI Interface Configuration Register (Default Value: 0x00000000)

| Offset: 0x0004 | | | Register Name: CSI0_IF_CFG_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| 27:24 | R/W | 0x1 | FIELD_DT_PCLK_SHIFT Only for vsync detected field mode,the odd field permitted pclk shift = 4* FIELD_DT_PCLK_SHIFT |
| 23:22 | / | / | / |
| 21 | R/W | 0x0 | SRC_TYPE Source type 0: Progressed 1: Interlaced |
| 20 | R/W | 0x0 | FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames |

| | | | |
|-------|-----|-----|--|
| 19 | R/W | 0x0 | FIELD For YUV HV timing, Field polarity 0: negative(field=0 indicate odd, field=1 indicate even) 1: positive(field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first) |
| 18 | R/W | 0x1 | VREF_POL Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface. |
| 17 | R/W | 0x0 | HERF_POL Href polarity 0: negative 1: positive This register is not apply to CCIR656 interface. |
| 16 | R/W | 0x1 | CLK_POL Data clock type 0: active in rising edge 1: active in falling edge |
| 15:14 | R/W | 0x0 | Field_DT_MODE (only valid when CSI_IF is YUV and source type is interlaced) 00:by both field and vsync 01:by field 10:by vsync 11:reserved |
| 13 | / | / | / |
| 12:11 | R/W | 0x0 | SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D[11:4] will be rearranged to D[11:2]+2'b0 at the actual csi data bus according to these sequences: 00: 6'bx+D[9:8], D[7:0] 01: D[9:2], 6'bx+D[1:0] 10: D[7:0], D[9:8]+6'bx 11: D[7:0], 6'bx+D[9:8] |
| 10:8 | R/W | 0x0 | IF_DATA_WIDTH 000: 8 bit data bus 001: 10 bit data bus 010: 12 bit data bus 011: 8+2bit data bus 100:2x8bit data bus Other:reserved |
| 7 | R/W | 0x0 | MIPI_IF MIPI Interface Enable: 0: CSI 1: MIPI |
| 6:5 | / | / | / |
| 4:0 | R/W | 0x0 | CSI_IF YUV: 00000: YUYV422 Interleaved or RAW (All data in one data bus) 00001: YUV422 UV Combined (16 bit interface with seperate syncs) CCIR656: |

| | | | |
|--|--|--|--|
| | | | 00100: YUYV422 Interleaved or RAW (All data in one data bus) 00101: YUV422 UV Combined (16 bit inrerface with embedded syncs, BT1120) Others: Reserved |
|--|--|--|--|

6.1.4.3. CSI Capture Register (Default Value: 0x00000000)

| Offset: 0x0008 | | | Register Name: CSIO_CAP_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:6 | / | / | / |
| 5:2 | R/W | 0x0 | CH0_CAP_MASK Vsync number masked before capture. |
| 1 | R/W | 0x0 | CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame. |
| 0 | R/W | 0x0 | CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0. |

6.1.4.4. CSI Synchronization Counter Register (Default Value: 0x00000000)

| Offset: 0x000C | | | Register Name: CSIO_SYNC_CNT_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:0 | R | 0x0 | SYNC_CNT The counter value between vsync of CSIO channel 0 and vsync of CSIO channel 0, using 24MHz. |

6.1.4.5. CSI FIFO Threshold Register (Default Value: 0x040f0400)

| Offset: 0x0010 | | | Register Name: CSIO_FIFO_THRS_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:26 | R/W | 0x1 | FIFO_NEARLY_FULL_TH The threshold of FIFO being nearly full. Indicates that the ISP should stop writing. Only valid when ISP is enabled. 0~7: The smaller the value, the flag of FIFO being nearly full is easier to reach. |
| 25:24 | R/W | 0x0 | PTN_GEN_CLK_DIV Packet generator clock divider |

| | | | |
|-------|-----|-------|--|
| 23:16 | R/W | 0x0f | PTN_GEN_DLY Clocks delayed before pattern generating start. |
| 15:12 | / | / | / |
| 11:00 | R/W | 0x400 | FIFO_THRS When CSIO FIFO occupied memory exceed the threshold, dram frequency can not change. |

6.1.4.6. CSI BT656 Header Configuration Register (Default Value: 0x03020100)

| Offset: 0x0014 | | | Register Name: CSIO_BT656_HEAD_CFG_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| 27:24 | R/W | 0x3 | CH3_ID The low 4bit of BT656 header for channel 3 Only valid in BT656 multi-channel mode |
| 23:20 | / | / | / |
| 19:16 | R/W | 0x2 | CH2_ID The low 4bit of BT656 header for channel 2 Only valid in BT656 multi-channel mode |
| 15:12 | / | / | / |
| 11:08 | R/W | 0x1 | CH1_ID The low 4bit of BT656 header for channel 1 Only valid in BT656 multi-channel mode |
| 07:04 | / | / | / |
| 03:00 | R/W | 0x0 | CH0_ID The low 4bit of BT656 header for channel 0 Only valid in BT656 multi-channel mode |

6.1.4.7. CSI Pattern Generation Length Register (Default Value: 0x00000000)

| Offset: 0x0030 | | | Register Name: CSIO_PTN_LEN_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | PTN_LEN The pattern length in byte when generating pattern. |

6.1.4.8. CSI Pattern Generation Address Register (Default Value: 0x00000000)

| Offset: 0x0034 | | | Register Name: CSIO_PTN_ADDR_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | PTN_ADDR The pattern DRAM address when generating pattern. |

6.1.4.9. CSI Version Register(Default Value: 0x00000000)

| Offset: 0x003C | | | Register Name: CSIO_VER_REG |
|----------------|-----|-------------|------------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | / | VER |

| | | | |
|--|--|--|--|
| | | | Version of hardware circuit. Only can be read when version register read enable is on. |
|--|--|--|--|

6.1.4.10. CSI Channel_0 configuration Register (Default Value: 0x00300200)

| Offset: 0x0044 | | | Register Name: CSIO_CO_CFG_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:24 | R/W | 0x0 | PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff |
| 23:20 | R/W | 0x3 | INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved |
| 19:16 | R/W | 0x0 | OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved |

| | | | |
|-------|-----|-----|---|
| | | | When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved Others: reserved |
| 15:14 | / | / | / |
| 13 | R/W | 0x0 | VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable |
| 12 | R/W | 0x0 | HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable |
| 11:10 | R/W | 0x0 | FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved |
| 09:08 | R/W | 0x2 | INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU |
| 07:02 | / | / | / |
| 01:00 | R/W | 0x0 | MIN_SDR_WR_SIZE Minimum size of SDRAM block write 0: 256 bytes (if hflip is enable, always select 256 bytes) 1: 512 bytes 2: 1k bytes 3: 2k bytes |

6.1.4.11. CSI Channel_0 scale Register (Default Value: 0x00000000)

| Offset: 0x004C | | | Register Name: CSIO_CO_SCALE_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:01 | / | / | / |
| 00 | R/W | 0x0 | QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported. |

6.1.4.12. CSI Channel_0 FIFO 0 output buffer-A address Register (Default Value: 0x00000000)

| Offset: 0x0050 | | | Register Name: CSIO_CO_F0_BUFA_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:00 | R/W | 0x0 | COF0_BUFA FIFO 0 output buffer-A address |

6.1.4.13. CSI Channel_0 FIFO 1 output buffer-A address Register (Default Value: 0x00000000)

| Offset: 0x0058 | | | Register Name: CSIO_CO_F1_BUFA_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:00 | R/W | 0x0 | COF1_BUFA FIFO 1 output buffer-A address |

6.1.4.14. CSI Channel_0 FIFO 2 output buffer-A address Register (Default Value: 0x00000000)

| Offset: 0x0060 | | | Register Name: CSIO_CO_F2_BUFA_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:00 | R/W | 0x0 | COF2_BUFA FIFO 2 output buffer-A address |

6.1.4.15. CSI Channel_0 status Register (Default Value: 0x00000000)

| Offset: 0x006C | | | Register Name: CSIO_CO_CAP_STA_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:03 | / | / | / |
| 02 | R | 0x0 | FIELD_STA The status of the received field 0: Field 0 1: Field 1 |
| 01 | R | 0x0 | VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured. |

| | | | |
|----|---|-----|--|
| 00 | R | 0x0 | <p>SCAP_STA</p> <p>Still capture in progress</p> <p>Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured.</p> <p>For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.</p> |
|----|---|-----|--|

6.1.4.16. CSI Channel_0 interrupt enable Register (Default Value: 0x00000000)

| Offset: 0x0070 | | | Register Name: CSIO_CO_INT_EN_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:08 | / | / | / |
| 07 | R/W | 0x0 | <p>VS_INT_EN</p> <p>vsync flag</p> <p>The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame</p> |
| 06 | R/W | 0x0 | <p>HB_OF_INT_EN</p> <p>Hblank FIFO overflow</p> <p>The bit is set when 3 FIFOs still overflow after the hblank.</p> |
| 05 | R/W | 0x0 | <p>MUL_ERR_INT_EN</p> <p>Multi-channel writing error</p> <p>Indicates error has been detected for writing data to a wrong channel.</p> |
| 04 | R/W | 0x0 | <p>FIFO2_OF_INT_EN</p> <p>FIFO 2 overflow</p> <p>The bit is set when the FIFO 2 become overflow.</p> |
| 03 | R/W | 0x0 | <p>FIFO1_OF_INT_EN</p> <p>FIFO 1 overflow</p> <p>The bit is set when the FIFO 1 become overflow.</p> |
| 02 | R/W | 0x0 | <p>FIFO0_OF_INT_EN</p> <p>FIFO 0 overflow</p> <p>The bit is set when the FIFO 0 become overflow.</p> |
| 01 | R/W | 0x0 | <p>FD_INT_EN</p> <p>Frame done</p> <p>Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is writed to buffer as long as video capture remains enabled.</p> |
| 00 | R/W | 0x0 | <p>CD_INT_EN</p> <p>Capture done</p> <p>Indicates the CSI has completed capturing the image data.</p> <p>For still capture, the bit is set when one frame data has been wrote to buffer.</p> <p>For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled.</p> <p>For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.</p> |

6.1.4.17. CSI Channel_0 interrupt status Register (Default Value: 0x00000000)

| | |
|----------------|------------------------------------|
| Offset: 0x0074 | Register Name: CSIO_CO_INT_STA_REG |
|----------------|------------------------------------|

| Bit | R/W | Default/Hex | Description |
|-------|-----|-------------|---|
| 31:08 | / | / | / |
| 07 | R/W | 0x0 | VS_PD vsync flag |
| 06 | R/W | 0x0 | HB_OF_PD Hblank FIFO overflow |
| 05 | R/W | 0x0 | MUL_ERR_PD Multi-channel writing error |
| 04 | R/W | 0x0 | FIFO2_OF_PD FIFO 2 overflow |
| 03 | R/W | 0x0 | FIFO1_OF_PD FIFO 1 overflow |
| 02 | R/W | 0x0 | FIFO0_OF_PD FIFO 0 overflow |
| 01 | R/W | 0x0 | FD_PD Frame done |
| 00 | R/W | 0x0 | CD_PD Capture done |

6.1.4.18. CSI Channel_0 filed1 vertical size Register (Default Value: 0x01E00000)

| Offset: 0x0078 | | | Register Name: CSIO_CO_FLD1_VSIZE_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:16 | R/W | 0x1E0 | VER_LEN Valid line number of filed1, only valid when CSI_IF is YUV and source type is interlaced. |
| 15:13 | / | / | / |
| 12:00 | R/W | 0x0 | VER_START Vertical line start of filed1. data is valid from this line, only valid when CSI_IF is YUV and source type is interlaced. |

6.1.4.19. CSI Channel_0 horizontal size Register (Default Value: 0x05000000)

| Offset: 0x0080 | | | Register Name: CSIO_CO_INT_STA_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:16 | R/W | 0x500 | HOR_LEN Horizontal pixel unit length. Valid pixel of a line. |
| 15:13 | / | / | / |
| 12:00 | R/W | 0x0 | HOR_START Horizontal pixel unit start. Pixel is valid from this pixel. |

6.1.4.20. CSI Channel_0 vertical size Register (Default Value: 0x01E00000)

| Offset: 0x0084 | | | Register Name: CSIO_CO_VSIZE_REG |
|----------------|-----|-------------|----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |

| | | | |
|-------|-----|-------|--|
| 28:16 | R/W | 0x1E0 | VER_LEN Vertical line length. Valid line number of a frame. Stand for line number of field0 when CSI_IF is YUV and source type is interlaced. |
| 15:13 | / | / | / |
| 12:00 | R/W | 0x0 | VER_START Vertical line start. data is valid from this line. Stand for start line of field0 when CSI_IF is YUV and source type is interlaced. |

6.1.4.21. CSI Channel_0 buffer length Register (Default Value: 0x01400280)

| Offset: 0x0088 | | | Register Name: CSIO_CO_BUF_LEN_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:30 | / | / | / |
| 29:16 | R/W | 0x140 | BUF_LEN_C Buffer length of chroma C in a line. Unit is byte. |
| 15:14 | / | / | / |
| 13:00 | R/W | 0x280 | BUF_LEN Buffer length of luminance Y in a line. Unit is byte. |

6.1.4.22. CSI Channel_0 flip size Register (Default Value: 0x01E00280)

| Offset: 0x008C | | | Register Name: CSIO_CO_FLIP_SIZE_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:16 | R/W | 0x1E0 | VER_LEN Vertical line number when in vflip mode. |
| 15:13 | / | / | / |
| 12:00 | R/W | 0x280 | VALID_LEN Valid components of a line when in flip mode. |

6.1.4.23. CSI Channel_0 frame clock counter Register (Default Value: 0x00000000)

| Offset: 0x0090 | | | Register Name: CSIO_CO_FRM_CLK_CNT_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:00 | R | 0x0 | FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0. |

6.1.4.24. CSI Channel_0 accumulated and internal clock counter Register (Default Value: 0x00000000)

| Offset: 0x0094 | | | Register Name: CSIO_CO_ACC_ITNL_CLK_CNT_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:24 | R | 0x0 | ACC_CLK_CNT |

| | | | |
|-------|---|-----|--|
| | | | <p>The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame.</p> <p>When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.</p> |
| 23:00 | R | 0x0 | <p>ITNL_CLK_CNT</p> <p>The instant value of internal frame clock counter.</p> <p>When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.</p> |

6.1.4.25. CSI Channel_0 FIFO Statistic Register (Default Value: 0x00000000)

| Offset: 0x0098 | | | Register Name: CSIO_CO_FIFO_STAT_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:12 | / | / | / |
| 11:00 | R | 0x0 | <p>FIFO_FRM_MAX</p> <p>Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or framedone.</p> |

6.1.4.26. CSI Channel_0 PCLK Statistic Register (Default Value: 0x00007FFF)

| Offset: 0x009C | | | Register Name: CSIO_CO_PCLK_STAT_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30:16 | R | 0x0 | <p>PCLK_CNT_LINE_MAX</p> <p>Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.</p> |
| 15 | / | / | / |
| 14:00 | R | 0x7fff | <p>PCLK_CNT_LINE_MIN</p> <p>Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.</p> |

6.1.4.27. CCI Control Register (Default Value: 0x00000000)

| Offset: 0x3000 | | | Register Name: CCI_CTRL_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | <p>SINGLE_TRAN</p> <p>0: Transmission idle</p> <p>1: Start single transmission</p> <p>Automatically cleared to '0' when finished. Abort current transmission immediately if changing from '1' to '0'. If slave not respond for the expected status over the time defined by TIMEOUT, current transmission will stop. PACKET_CNT will return the sequence number when transmission fail. All format setting and data will be loaded from registers and FIFO when transmission start.</p> |
| 30 | R/W | 0x0 | <p>REPEAT_TRAN</p> <p>0: transmission idle</p> |

| | | | |
|-------|-----|-----|--|
| | | | 1: repeated transmission When this bit is set to 1, transmission repeats when trigger signal (such as VSYNC/ VCAP done) repeats. If changing this bit from '1' to '0' during transmission, the current transmission will be guaranteed then stop. |
| 29 | R/W | 0x0 | RESTART_MODE 0: RESTART 1: STOP+START Define the CCI action after sending register address. |
| 28 | R/W | 0x0 | READ_TRAN_MODE 0: send slave_id+W 1: do not send slave_id+W Setting this bit to 1 if reading from a slave which register width is equal to 0. |
| 27:24 | R | 0x0 | TRAN_RESULT 000: OK 001: FAIL Other: Reserved |
| 23:16 | R | / | CCI_STA 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending 9th SCL clk Other: Reserved |
| 15:2 | / | / | / |
| 1 | R/W | 0x0 | SOFT_RESET 0: normal 1: reset |
| 0 | R/W | 0x0 | CCI_EN 0: Module disable 1: Module enable |

6.1.4.28. CCI Transmission Configuration Register (Default Value: 0x10000000)

| Offset: 0x3004 | | | Register Name: CCI_CFG_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:24 | R/W | 0x10 | TIMEOUT_N When sending the 9th clock, assert fail signal when slave device did not response after N*FSCL cycles. And software must do a reset to CCI module and send a stop condition to slave. |
| 23:16 | R/W | 0x00 | INTERVAL Define the interval between each packet in 40*FSCL cycles. 0~255 |
| 15 | R/W | 0x0 | PACKET_MODE Select where to load slave id / data width |

| | | | |
|------|-----|-----|---|
| | | | 0: Compact mode 1: Complete mode In compact mode, slave id/register width / data width will be loaded from CCI_FMT register, only address and data read from memory. In complete mode, they will be loaded from packet memory. |
| 14:7 | / | / | / |
| 6:4 | R/W | 0x0 | TRIG_MODE Transmit mode: 000: Immediately, no trigger 001: Reserved 010: CSIO int trigger 011: CSI1 int trigger |
| 3:0 | R/W | 0x0 | CSI_TRIG CSI Int trig signal select: 0000: First HREF start 0001: Last HREF done 0010: Line counter trigger other: Reserved |

6.1.4.29. CCI Packet Format Register (Default Value: 0x00110001)

| Offset: 0x3008 | | | Register Name: CCI_FMT_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:25 | R/W | 0x0 | SLV_ID 7bit address |
| 24 | R/W | 0x0 | CMD 0: write 1: read |
| 23:20 | R/W | 0x1 | ADDR_BYTE How many bytes be sent as address 0~15 |
| 19:16 | R/W | 0x1 | DATA_BYTE How many bytes be sent/received as data 1~15 Normally use ADDR_DATA with 0_2, 1_1, 1_2, 2_1, 2_2 access mode. If DATA bytes is 0, transmission will not start. In complete mode, the ADDR_BYTE and DATA_BYTE is defined in a byte's high/low 4bit. |
| 15:0 | R/W | 0x1 | PACKET_CNT FIFO data be transmitted as PACKET_CNT packets in current format. Total bytes not exceed 32bytes. |

6.1.4.30. CCI Bus Control Register (Default Value: 0x00002500)

| Offset: 0x300C | | | Register Name: CCI_BUS_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | R/W | 0x0 | DLY_CYC 0~65535 FSCL cycles between each transmission |
| 15 | R/W | 0x0 | DLY_TRIG 0: disable 1: execute transmission after internal counter delay when triggered |
| 14:12 | R/W | 0x2 | CLK_N |

| | | | |
|------|-----|-----|--|
| | | | CCI bus sampling clock $F_0=24\text{MHz}/2^{\wedge}\text{CLK_N}$ |
| 11:8 | R/W | 0x5 | CLK_M CCI output SCL frequency is $\text{FSCL}=F_1/10=(F_0/(\text{CLK_M}+1))/10$ |
| 7 | R | / | SCL_STA SCL current status |
| 6 | R | / | SDA_STA SDA current status |
| 5 | R/W | 0x0 | SCL_PEN SCL PAD enable |
| 4 | R/W | 0x0 | SDA_PEN SDA PAD enable |
| 3 | R/W | 0x0 | SCL_MOV SCL manual output value |
| 2 | R/W | 0x0 | SDA_MOV SDA manual output value |
| 1 | R/W | 0x0 | SCL_MOE SCL manual output en |
| 0 | R/W | 0x0 | SDA_MOE SDA manual output en |

6.1.4.31. CCI Interrupt Control Register (Default Value: 0x00000000)

| Offset: 0x3014 | | | Register Name: CCI_INT_CTRL_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:18 | / | / | / |
| 17 | R/W | 0x0 | S_TRAN_ERR_INT_EN |
| 16 | R/W | 0x0 | S_TRAN_COM_INT_EN |
| 15:2 | / | / | / |
| 1 | R/W | 0x0 | S_TRAN_ERR_PD |
| 0 | R/W | 0x0 | S_TRAN_COM_PD |

6.1.4.32. CCI Line Counter Trigger Control Register (Default Value: 0x00000000)

| Offset: 0x3018 | | | Register Name: CCI_LC_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:13 | / | / | / |
| 12:0 | R/W | 0x0 | LN_CNT 0~8191: line counter send trigger when 1st~8192th line is received. |

6.1.4.33. CCI FIFO Access Register (Default Value: 0x00000000)

| Offset: 0x3100~0x313f | | | Register Name: CCI_FIFO_ACC_REG |
|-----------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0x0 | DATA_FIFO From 0x100 to 0x13f, CCI data fifo is 64bytes, used in fifo input mode. CCI transmission read/write data from/to fifo in byte. |

6.2. MIPI CSI2

6.2.1. Overview

The MIPI CSI2 includes the following feature:

- MIPI CSI-2 Receiver as a slave without CCI (Camera Control Interface)
- Unidirectional Clock and Data Lane
- Standard CSI-2 protocol with ECC and CRC
- Supports format: YUV422-8bit/10bit, YUV420-8bit/10bit, RAW-8, RAW-10, RAW-12, RGB888, RGB565
- D-PHY with HS-RX, LP-TX, LP-RX
- 1,2,3,4 Data Lanes Configuration and up to 1Gbps per Lane in HS Transmission
- Maximum to 720p@30fps or 1080p@15fps with one data Lane in one channel
- Maximum to 1080p@30fps or 5M@15fps with two data Lanes in one channel
- Maximum to 1080p@60fps or 8M@24fps with four data Lanes in one channel
- Maximum to 4 data type interleaving in one channel

Chapter 7 Display

This chapter describes the S3 display system from two aspects:

- DE2.0
- TCON

The following figure shows the block diagram of display system:

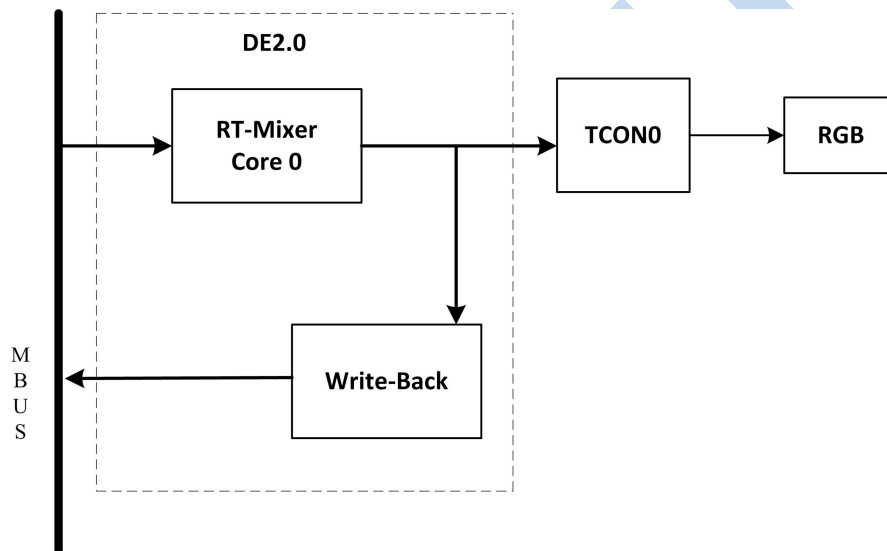


Figure 7-1. Display System Block Diagram

7.1. DE 2.0

7.1.1. Overview

- Output size up to 1024x1024
- Support three alpha blending channel for main display
- Support four overlay layers in each channel, and has a independent scale
- Support potter-duff compatible blending operation
- Support input format YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB 565

7.2. TCON

7.2.1. Overview

- Support LVDS interface with single link, up to 1024x768@60fps
- Support RGB interface with DE/SYNC mode, up to 1024x768@60fps
- Support serial RGB/dummy RGB/CCIR656 interface, up to 800x480@60fps
- Support i80 interface with 18/16/9/8 bit, support TE, up to 800x480@60fps
- Support pixel format: RGB888, RGB666 and RGB565
- Dither function from RGB666/RGB565 to RGB888
- Gamma correction with R/G/B channel independence
- 4 interrupts for programmer LCD output

7.2.2. Block Diagram

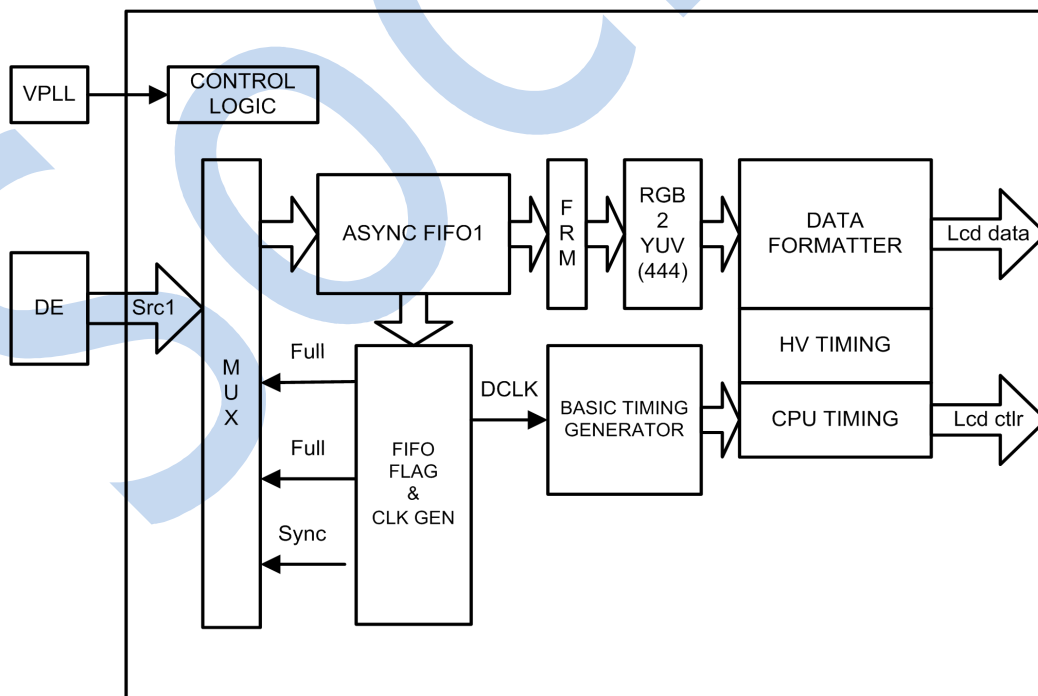


Figure 7-2. TCON Block Diagram

7.2.3. Functionalities Description

7.2.3.1. Panel Interface

HV_I/F(Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications. Its signals are define as:

| Main Signal | I/O type | Definition And Description |
|-------------|----------|--|
| Vsync | O | Vertical sync, indicates one new frame |
| Hsync | O | Horizontal sync, indicate one new scan line |
| DCLK | O | Dot clock, pixel data are sync by this clock |
| LDE | O | LCD data enable |
| LD[23..0] | O | 18Bit RGB/YUV output from input FIFO for panel |

HV control signals are active low.

Vertical Timing

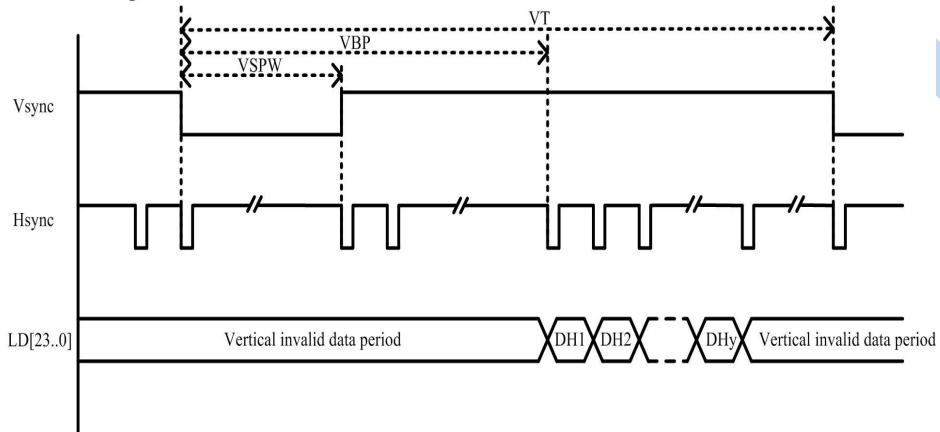


Figure 7-3. Panel Interface Odd/Even Field Vertical Timing

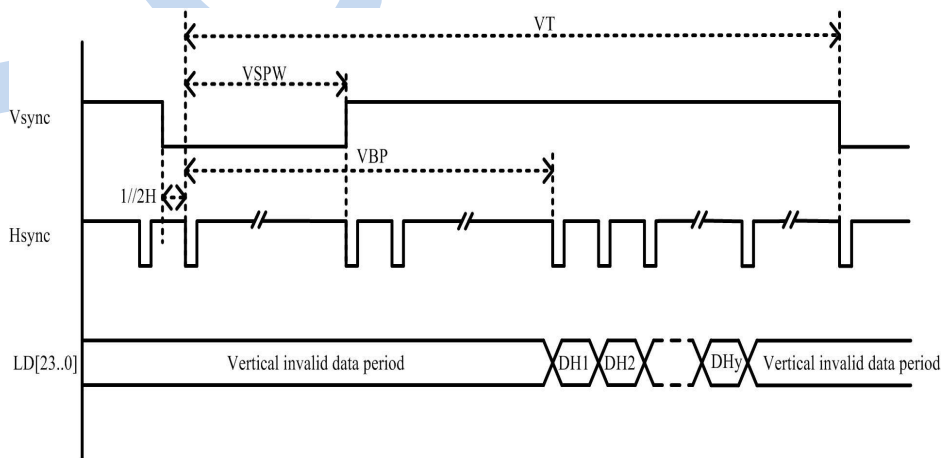


Figure 7-4. Panel Interface Even Field Vertical Timing

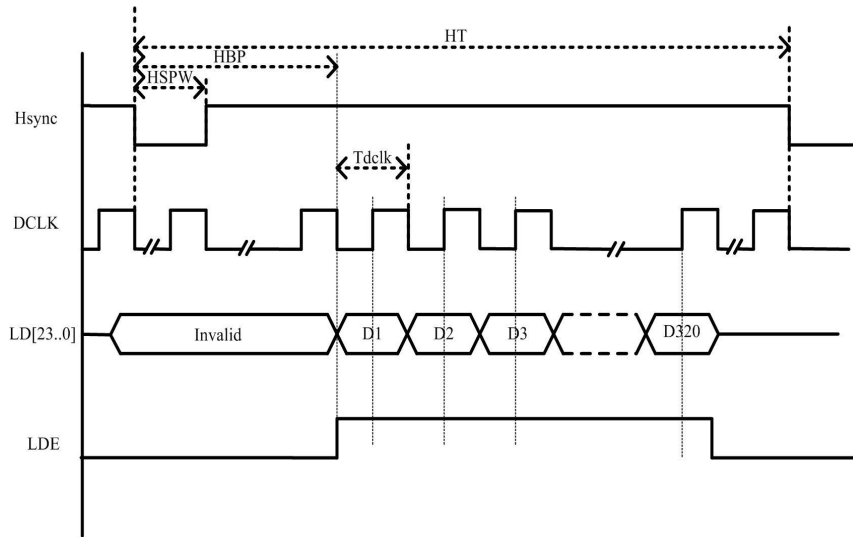


Figure 7-5. Parallel Mode Horizontal Timing

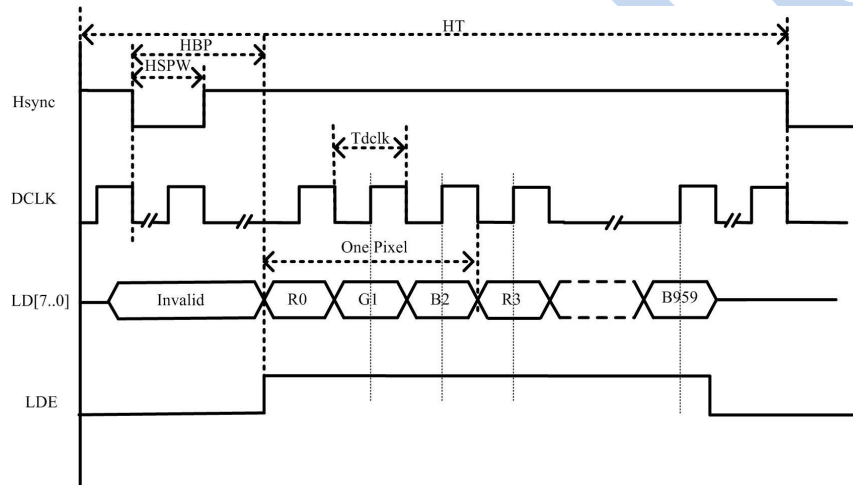


Figure 7-6. Serial Mode Horizontal Timing

CCIR output SAV/EAV sync signal

When in HV serial YUV output mode, it's timing is CCIR656/601 compatible. SAV add right before active area every line; EAV add right after active area every line.

It logic are:

F = "0" for Field 1 F = "1" for Field 2

V = "1" during vertical blanking

H = "0" at SAV H = "1" at EAV

P3-P0 = protection bits

$$P3 = V \oplus H$$

$$P2 = F \oplus H$$

$$P1 = F \oplus V$$

$$P0 = F \oplus V \oplus H$$

Where \oplus represents the exclusive-OR function

The 4 byte SAV/EAV sequences are:

| | | |
|--|------------|-------------|
| | 8-bit Data | 10-bit Data |
|--|------------|-------------|

| | | | | | | | | | | |
|-------------|----------|----|----|----|----|----|----|----|----|----|
| | D9 (MSB) | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| preamble | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Status word | 1 | F | V | H | P3 | P2 | P1 | P0 | 0 | 0 |

CPU_I/F

CPU I/F LCD panel is most common interface for small size, low resolution LCD panels. CPU control signals are active low.

| Main Signal | I/O type | Definition And Description |
|-------------|----------|--|
| CS | O | Chip select, active low |
| WR | O | Write strobe, active low |
| RD | O | Read strobe, active low |
| A1 | O | Address bit, controlled by "LCD_CPUI/F" BIT26/25 |
| D[23..0] | I/O | Digital RGB output signal |

The following figure relationship between basic timing and CPU timing. WR is 180 degree delay of DCLK; CS is active when pixel data are valid; RD is always set to 1; A1 are set by "Lcd_CPUI/F".

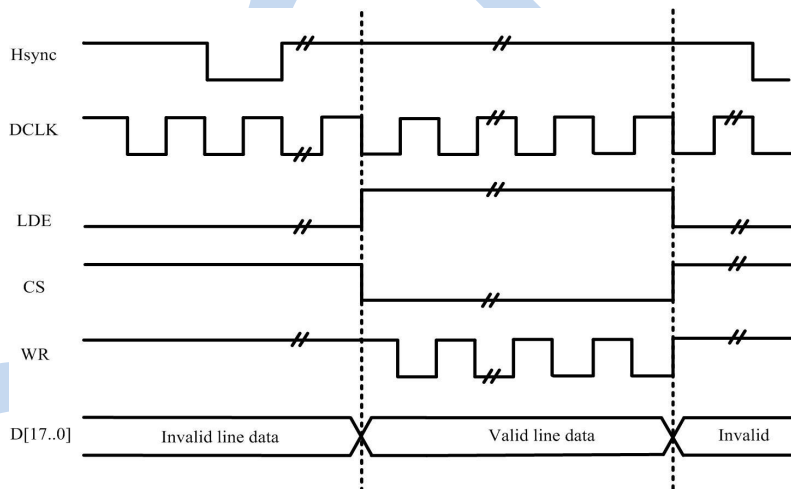


Figure 7-7. Lcd_CPUI/F Timing

When CPU I/F is in IDLE state, it can generate WR/RD timing by setting "Lcd_CPUI/F". CS strobe is one DCLK width, WR/RD strobe is half DCLK width.

LVDS_IF

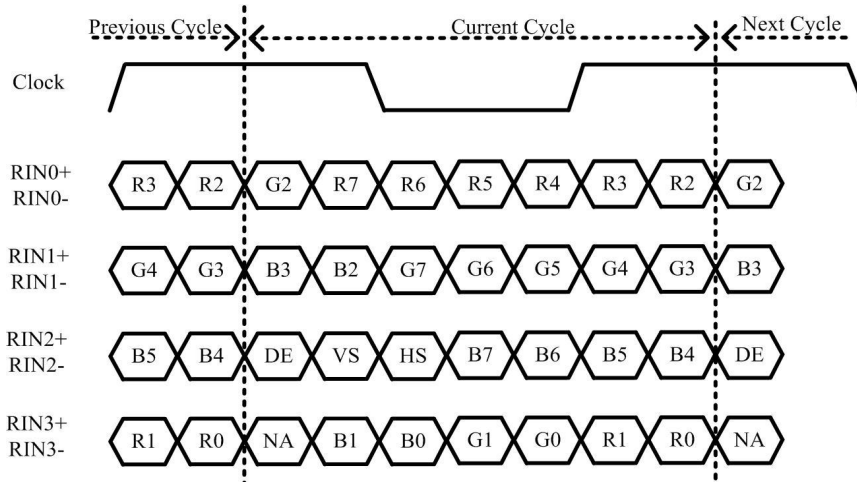


Figure 7-8. JEDIA Mode Timing

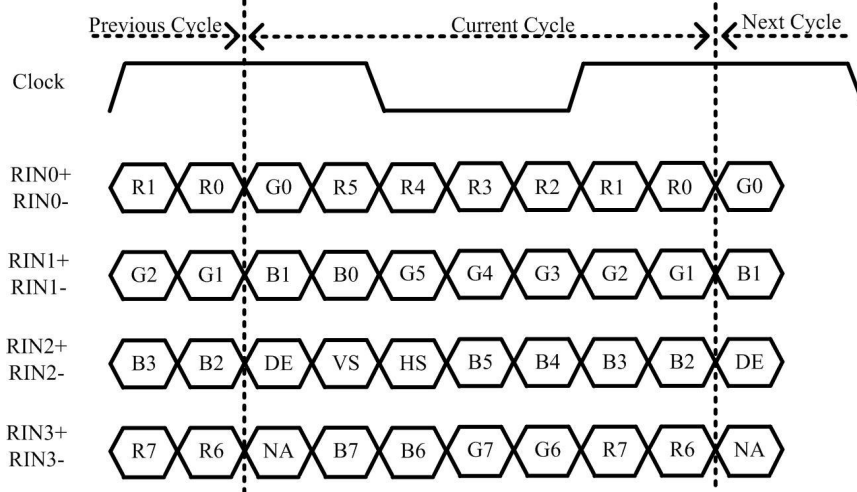


Figure 7-9. NS Mode Timing

7.2.3.2. RGB gamma correction

Function: This module correct the RGB input data of DE0 .

A 256*8*3 Byte register file is used to store the gamma table. The following is the layout:

| Offset | Value |
|---------------------|-------------------------------------|
| 0x400, 0x401, 0x402 | { B0[7:0], G0[7:0], R0[7:0] } |
| 0x404, | { B1[7:0], G1[7:0], R1[7:0] } |
| | |
| 0x4FC | { B255[7:0], G255[7:0], R255[7:0] } |

7.2.3.3. CEU module

Function: This module enhance color data from DE0 .

$$R' = Rr * R + Rg * G + Rb * B + Rc$$

$$G' = Gr * R + Gg * G + Gb * B + Gc$$

$$B' = Br * R + Bg * G + Bb * B + Bc$$

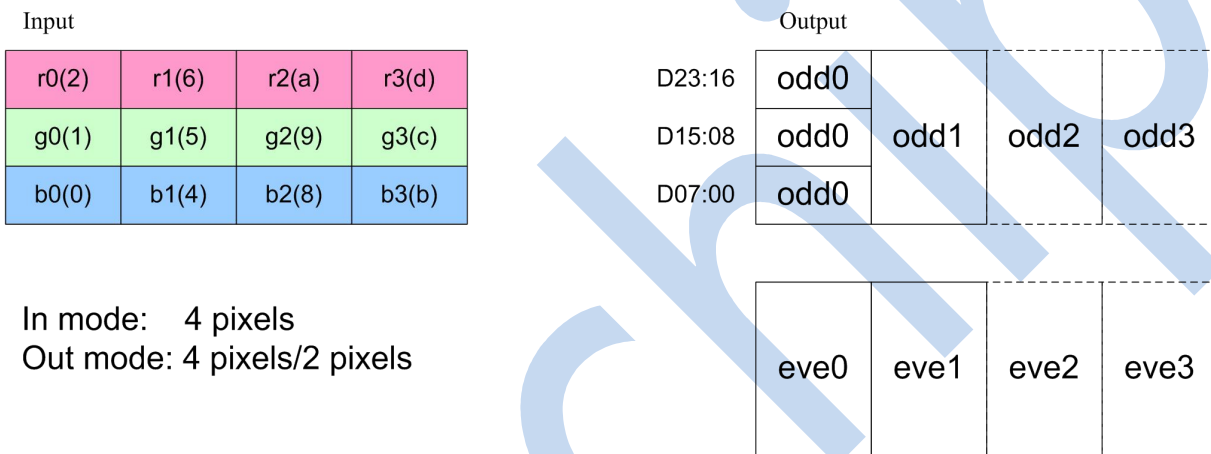
Note:

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb s13 (-16,16)
 Rc, Gc, Bc s19 (-16384, 16384)
 R, G, B u8 [0-255]
 R' have the range of [Rmin ,Rmax]
 G' have the range of [Rmin ,Rmax]
 B' have the range of [Rmin ,Rmax]

7.2.3.4. CMAP module

Function: This module map color data from DE0

Every 4 input pixels as an unit. an unit is divided into 12 bytes. Output byte can select one of those 12 bytes. Note that even line and odd line can be different, and output can be 12 bytes(4 pixels) or reduce to 6 bytes(2 pixels).



In mode: 4 pixels
 Out mode: 4 pixels/2 pixels

7.2.4. TCON Module Register List

| Module Name | Base Address |
|-------------|--------------|
| TCON | 0x01C0C000 |

| Register Name | Offset | Description |
|--------------------|--------------|--|
| TCON_GCTL_REG | 0x000 | TCON global control register |
| TCON_GINT0_REG | 0x004 | TCON global interrupt register0 |
| TCON_GINT1_REG | 0x008 | TCON global interrupt register1 |
| TCON0_FRM_CTL_REG | 0x010 | TCON FRM control register |
| TCON0_FRM_SEED_REG | 0x014+N*0x04 | TCON FRM seed register (N=0,1,2,3,4,5) |
| TCON0_FRM_TAB_REG | 0x02C+N*0x04 | TCON FRM table register (N=0,1,2,3) |
| TCON0_CTL_REG | 0x040 | TCON0 control register |
| TCON0_DCLK_REG | 0x044 | TCON0 data clock register |
| TCON0_BASIC0_REG | 0x048 | TCON0 basic timing register0 |
| TCON0_BASIC1_REG | 0x04C | TCON0 basic timing register1 |
| TCON0_BASIC2_REG | 0x050 | TCON0 basic timing register2 |
| TCON0_BASIC3_REG | 0x054 | TCON0 basic timing register3 |
| TCON0_HV_IF_REG | 0x058 | TCON0 hv panel interface register |
| TCON0_CPU_IF_REG | 0x060 | TCON0 cpu panel interface register |

| | | |
|------------------------|--------------|--|
| TCON0_CPU_WR_REG | 0x064 | TCON0 cpu panel write data register |
| TCON0_CPU_RD0_REG | 0x068 | TCON0 cpu panel read data register0 |
| TCON0_CPU_RD1_REG | 0x06C | TCON0 cpu panel read data register1 |
| TCON0_LVDS_IF_REG | 0x084 | TCON0 lvds panel interface register |
| TCON0_IO_POL_REG | 0x088 | TCON0 IO polarity register |
| TCON0_IO_TRI_REG | 0x08C | TCON0 IO control register |
| TCON_ECC_FIFO_REG | 0x0F8 | TCON ECC FIFO register |
| TCON_DEBUG_REG | 0x0FC | TCON debug register |
| TCON_CEU_CTL_REG | 0x100 | TCON CEU control register |
| TCON_CEU_COEF_MUL_REG | 0x110+N*0x04 | TCON CEU coefficient register0 (N=0,1,2,4,5,6,8,9,10) |
| TCON_CEU_COEF_ADD_REG | 0x11C+N*0x10 | TCON CEU coefficient register1 (N=0,1,2) |
| TCON_CEU_COEF_RANG_REG | 0x140+N*0x04 | TCON CEU coefficient register2 (N=0,1,2) |
| TCON0_CPU_TRI0_REG | 0x160 | TCON0 cpu panel trigger register0 |
| TCON0_CPU_TRI1_REG | 0x164 | TCON0 cpu panel trigger register1 |
| TCON0_CPU_TRI2_REG | 0x168 | TCON0 cpu panel trigger register2 |
| TCON0_CPU_TRI3_REG | 0x16C | TCON0 cpu panel trigger register3 |
| TCON_CMAP_CTL_REG | 0x180 | TCON color map control register |
| TCON_CMAP_ODD0_REG | 0x190 | TCON color map odd line register0 |
| TCON_CMAP_ODD1_REG | 0x194 | TCON color map odd line register1 |
| TCON_CMAP_EVEN0_REG | 0x198 | TCON color map even line register0 |
| TCON_CMAP_EVEN1_REG | 0x19C | TCON color map even line register1 |
| TCON_SAFE_PERIOD_REG | 0x1F0 | TCON safe period register |
| TCON0_LVDS_ANAO_REG | 0x220 | TCON LVDS analog register0 |
| TCON0_GAMMA_TABLE_REG | 0x400-0x7FF | |
| TCON_TRI_FIFO_BIST_REG | 0xFF8 | |
| TCON_ECC_FIFO_BIST_REG | 0xFFC | |

7.2.5. TCON Module Register Description

7.2.5.1. TCON_GCTL_REG (Default Value: 0x00000000)

| Offset: 0x0000 | | | Register Name: TCON_GCTL_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | TCON_En 0: disable 1: enable When it's disabled, the module will be reset to idle state. |
| 30 | R/W | 0 | TCON_Gamma_En 0: disable 1: enable |
| 29:0 | / | / | / |

7.2.5.2. TCON_GINT0_REG (Default Value: 0x00000000)

| Offset: 0x0004 | | | Register Name: TCON_GINT0_REG |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | TCON0_Vb_Int_En 0: disable 1: enable |
| 30 | / | / | / |
| 29 | R/W | 0 | TCON0_Line_Int_En 0: disable 1: enable |
| 28 | / | / | /1: enable |
| 27 | R/W | 0 | TCON0_Tri_Finish_Int_En 0: disable 1: enable |
| 26: | R/W | 0 | TCON0_Tri_Counter_Int_En 0: disable 1: enable |
| 25:16 | / | / | / |
| 15 | R/W | 0 | TCON0_Vb_Int_Flag Asserted during vertical no-display period every frame. Write 0 to clear it. |
| 14 | / | / | / |
| 13 | R/W | 0 | TCON0_Line_Int_Flag trigger when SY0 match the current TCON0 scan line Write 0 to clear it. |
| 12 | / | / | / |
| 11 | R/W | 0 | TCON0_Tri_Finish_Int_Flag trigger when cpu trigger mode finish Write 0 to clear it. |
| 10 | R/W | 0 | TCON0_Tri_Counter_Int_Flag trigger when tri counter reache this value Write 0 to clear it. |
| 9 | R/W | 0 | TCON0_Tri_Underflow_Flag only used in dsi video mode, tri when sync by dsi but not finish Write 0 to clear it. |
| 8:0 | / | / | / |

7.2.5.3. TCON_GINT1_REG (Default Value: 0x00000000)

| Offset: 0x0008 | | | Register Name: TCON_GINT1_REG |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| 27:16 | R/W | 0 | TCON0_Line_Int_Num Scan line for TCON0 line trigger(including inactive lines) Setting it for the specified line for trigger0. Note: SY0 is writable only when LINE_TRG0 disable. |
| 15:0 | / | / | / |

7.2.5.4. TCON0_TRM_CTL_REG (Default Value: 0x00000000)

| Offset: 0x010 | | | Register Name: TCON0_FRM_CTL_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | TCON0_Frm_En 0:disable 1:enable |
| 30:7 | / | / | / |
| 6 | R/W | 0 | TCON0_Frm_Mode_R 0: 6bit frm output 1: 5bit frm output |
| 5 | R/W | 0 | TCON0_Frm_Mode_G 0: 6bit frm output 1: 5bit frm output |
| 4 | R/W | 0 | TCON0_Frm_Mode_B 0: 6bit frm output 1: 5bit frm output |
| 3:2 | / | / | / |
| 1:0 | R/W | 0 | TCON0_Frm_Test 00: FRM 01: half 5/6bit, half FRM 10: half 8bit, half FRM 11: half 8bit, half 5/6bit |

7.2.5.5. TCON0_FRM_SEED_REG (Default Value: 0x00000000)

| Offset: 0x014+N*0x04 (N=0,1,2,3,4,5) | | | Register Name: TCON0_FRM_SEED_REG |
|---|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:25 | / | / | / |
| 24:0 | R/W | 0 | Seed_Value N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B Note: avoid set it to 0 |

7.2.5.6. TCON0_FRM_TAB_REG (Default Value: 0x00000000)

| Offset: 0x02C+N*0x04 (N=0,1,2,3) | | | Register Name: TCON0_FRM_TAB_REG |
|-------------------------------------|-----|-------------|----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | Frm_Table_Value |

7.2.5.7. TCON0_CTL_REG (Default Value: 0x00000000)

| Offset: 0x040 | | | Register Name: TCON0_CTL_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | TCON0_En 0: disable 1: enable Note: It executes at the beginning of the first blank line of TCON0 timing. |
| 30:29 | / | / | / |
| 28 | R/W | 0 | TCON0_Work_Mode 0: normal 1: dynamic freq |
| 27:26 | / | / | / |
| 25:24 | R/W | 0 | TCON0_IF 00: HV(Sync+DE) 01: 8080 I/F 1x:reserved |
| 23 | R/W | 0 | TCON0_RB_Swap 0: default 1: swap RED and BLUE data at FIFO1 |
| 22 | / | / | / |
| 21 | R/W | 0 | TCON0_FIFO1_Rst Write 1 and then 0 at this bit will reset FIFO 1 Note: 1 holding time must more than 1 DCLK |
| 20 | / | / | / |
| 19:9 | / | / | / |
| 8:4 | R/W | 0 | TCON0_Start_Delay STA delay NOTE: valid only when TCON0_EN == 1 |
| 3 | / | / | / |
| 2:0 | R/W | 0 | TCON0_SRC_SEL: 000: DE0 001: reserved 010: reserved 011: reserved 100: Test Data all 0 101: Test Data all 1 11x: reserved |

7.2.5.8. TCON0_DCLK_REG (Default Value: 0x00000000)

| Offset: 0x044 | | | Register Name: TCON0_DCLK_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | R/W | 0 | TCON0_Dclk_En LCLK_EN[3:0] :TCON0 clock enable 4'h0, 'h4,4'h6,4'ha7:dclk_en=0;dclk1_en=0;dclk2_en=0;dclkm2_en=0; 4'h1: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 4'h2: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 4'h3: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 4'h5: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 4'h8,4'h9,4'ha,4'hb,4'hc,4'hd,4'he,4'hf: dclk_en = 1; |

| | | | |
|------|-----|---|--|
| | | | dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1; |
| 27:7 | / | / | / |
| 6:0 | R/W | 0 | TCON0_Dclk_Div Tdclk = Tscclk * DCLKDIV Note: 1.if dclk1&dclk2 used, DCLKDIV >=6 2.if dclk only, DCLKDIV >=1 |

7.2.5.9. TCON0_BASIC0_REG (Default Value: 0x00000000)

| Offset: 0x048 | | | Register Name: TCON0_BASIC0_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| 27:16 | R/W | 0 | TCON0_X Panel width is X+1 |
| 15:12 | / | / | / |
| 11:0 | R/W | 0 | TCON0_Y Panel height is Y+1 |

7.2.5.10. TCON0_BASIC1_REG (Default Value: 0x00000000)

| Offset: 0x04C | | | Register Name: TCON0_BASIC1_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30:29 | / | / | / |
| 28:16 | R/W | 0 | HT Thcycle = (HT+1) * Tdclk Computation 1) parallel: HT = X + BLANK Limitation: 1) parallel :HT >= (HBP + 1) + (X+1) + 2 2) serial 1: HT >= (HBP + 1) + (X+1) * 3+2 3) serial 2: HT >= (HBP + 1) + (X+1) * 3/2+2 |
| 15:12 | / | / | / |
| 11:0 | R/W | 0 | HBP horizontal back porch (in dclk) Thbp = (HBP + 1) * Tdclk |

7.2.5.11. TCON0_BASIC2_REG (Default Value: 0x00000000)

| Offset: 0x050 | | | Register Name: TCON0_BASIC2_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:16 | R/W | 0 | VT TVT = (VT)/2 * Thsync Note: VT/2 >= (VBP+1) + (Y+1) + 2 |
| 15:12 | / | / | / |

| | | | |
|------|-----|---|---------------------------------|
| 11:0 | R/W | 0 | VBP Tvbp = (VBP +1) * Thsync |
|------|-----|---|---------------------------------|

7.2.5.12. TCON0_BASIC3_REG (Default Value: 0x00000000)

| Offset: 0x054 | | | Register Name: TCON0_BASIC3_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:26 | / | / | / |
| 25:16 | R/W | 0 | HSPW Thspw = (HSPW+1) * Tdclk Note: HT> (HSPW+1) |
| 15:10 | / | / | / |
| 9:0 | R/W | 0 | VSPW Tvspw = (VSPW+1) * Thsync Note: VT/2 > (VSPW+1) |

7.2.5.13. TCON0_HV_IF_REG (Default Value: 0x00000000)

| Offset: 0x058 | | | Register Name: TCON0_HV_IF_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | R/W | 0 | HV_Mode 0000: 24bit/1cycle parallel mode 1000: 8bit/3cycle RGB serial mode(RGB888) 1010: 8bit/4cycle Dummy RGB(DRGB) 1011: 8bit/4cycle RGB Dummy(RGBD) 1100: 8bit/2cycle YUV serial mode(CCIR656) |
| 27:26 | R/W | 0 | RGB888_SM0 serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7...) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B |
| 25:24 | R/W | 0 | RGB888_SM1 serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8...) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B |
| 23:22 | R/W | 0 | YUV_SM serial YUV mode Output sequence 2-pixel-pair of every scan line 00: YUYV 01: YVYU 10: UYYV 11: VYUY |
| 21:20 | R/W | 0 | YUV EAV/SAV F line delay 0:F toggle right after active video line 1:delay 2 line(CCIR PAL) 2:delay 3 line(CCIR NTSC) 3:reserved |

| | | | |
|------|---|---|---|
| 19:0 | / | / | / |
|------|---|---|---|

7.2.5.14. TCON0_CPU_IF_REG (Default Value: 0x00000000)

| Offset: 0x060 | | | Register Name: TCON0_CPU_IF_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | R/W | 0 | CPU_Mode 0000: 18bit/256K mode 0010: 16bit mode0 0100: 16bit mode1 0110: 16bit mode2 1000: 16bit mode3 1010: 9bit mode 1100: 8bit 256K mode 1110: 8bit 65K mode xxx1: 24bit for DSI |
| 27 | / | / | / |
| 26 | R/W | 0 | DA pin A1 value in 8080 mode auto/flash states |
| 25 | R/W | 0 | CA pin A1 value in 8080 mode WR/RD execute |
| 24 | / | / | / |
| 23 | R | 0 | Wr_Flag 0:write operation is finishing 1:write operation is pending |
| 22 | R | 0 | Rd_Flag 0:read operation is finishing 1:read operation is pending |
| 21:18 | / | / | / |
| 17 | R/W | 0 | AUTO auto Transfer Mode: If it's 1, all the valid data during this frame are write to panel. Note: This bit is sampled by Vsync |
| 16 | R/W | 0 | FLUSH direct transfer mode: If it's enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate control by DCLK. |
| 15:6 | / | / | / |
| 5:4 | R/W | 0 | / |
| 3 | R/W | 0 | Trigger_FIFO_Bist_En 0: disable 1: enable Entry addr is 0xFF8 |
| 2 | R/W | 0 | Trigger_FIFO_En 0:enable 1:disable |
| 1 | R/W | 0 | Trigger_Start write '1' to start a frame flush, write'0' has no effect. this flag indicated frame flush is running software must make sure write '1' only when this flag is '0'. |
| 0 | R/W | 0 | Trigger_En |

| | | | |
|--|--|--|---|
| | | | 0: trigger mode disable 1: trigger mode enable |
|--|--|--|---|

7.2.5.15. TCON0_CPU_WR_REG (Default Value: 0x00000000)

| Offset: 0x064 | | | Register Name: TCON0_CPU_WR_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:0 | W | 0 | Data_Wr data write on 8080 bus, launch a write operation on 8080 bus |

7.2.5.16. TCON0_CPU_RD0_REG (Default Value: 0x00000000)

| Offset: 0x068 | | | Register Name: TCON0_CPU_RD0_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:0 | R | / | Data_Rd0 data read on 8080 bus, launch a new read operation on 8080 bus |

7.2.5.17. TCON0_CPU_RD1_REG (Default Value: 0x00000000)

| Offset: 0x6C | | | Register Name: TCON0_CPU_RD1_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:0 | R | / | Data_Rd1 data read on 8080 bus, without a new read operation on 8080 bus |

7.2.5.18. TCON0_LVDS_IF_REG (Default Value: 0x00000000)

| Offset: 0x084 | | | Register Name: TCON0_LVDS_IF_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | TCON0_LVDS_En 0: disable 1: enable |
| 30 | / | / | / |
| 29 | R/W | 0 | TCON0_LVDS_Even_Odd_Dir 0: normal 1: reverse |
| 28 | R/W | 0 | TCON0_LVDS_Dir 1: normal 2: reverse NOTE: LVDS direction |
| 27 | R/W | 0 | TCON0_LVDS_Mode 0: NS mode 1: JEIDA mode |
| 26 | R/W | 0 | TCON0_LVDS_BitWidth 0: 24bit |

| | | | |
|-------|-----|---|---|
| | | | 1: 18bit |
| 25 | R/W | 0 | TCON0_LVDS_DeBug_En 0: disable 1: enable |
| 24 | R/W | 0 | TCON0_LVDS_DeBug_Mode 0: mode0 RANDOM DATA 1: mode1 output CLK period=7/2 LVDS CLK period |
| 23 | R/W | 0 | TCON0_LVDS_Correct_Mode 0: mode0 1: mode1 |
| 22:21 | / | / | / |
| 20 | R/W | 0 | TCON0_LVDS_Clk_Sel 0: MIPI PLL 1: TCON0 CLK |
| 19:5 | / | / | / |
| 4 | R/W | 0 | TCON0_LVDS_CLK_Polarity 0: reverse 1: normal |
| 3:0 | R/W | 0 | TCON0_LVDS_Data_Polarity 0: reverse 1: normal |

7.2.5.19. TCON0_IO_POL_REG (Default Value: 0x00000000)

| Offset: 0x88 | | | Register Name: TCON0_IO_POL_REG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | IO_Output_Sel 0: normal output 1: register output when set as '1', d[23:0], io0, io1,io3 sync to dclk |
| 30:28 | R/W | 0 | DCLK_Sel 000: used DCLK0(normal phase offset) 001: used DCLK1(1/3 phase offset) 010: used DCLK2(2/3 phase offset) 101: DCLK0/2 phase 0 100: DCLK0/2 phase 90 reserved |
| 27 | R/W | 0 | IO3_Inv 0: not invert 1: invert |
| 26 | R/W | 0 | IO2_Inv 0: not invert 1: invert |
| 25 | R/W | 0 | IO1_Inv 0: not invert 1: invert |
| 24 | R/W | 0 | IO0_Inv 0: not invert 1: invert |
| 23:0 | R/W | 0 | Data_Inv TCON0 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity |

| | | | |
|--|--|--|-------------------------------|
| | | | 1s: invert the specify output |
|--|--|--|-------------------------------|

7.2.5.20. TCON0_IO_TRI_REG (Default Value: 0x0FFFFFFF)

| Offset: 0x08C | | | Register Name: TCON0_IO_TRI_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28 | / | / | RGB_Endian 0: normal 1: bits_invert |
| 27 | R/W | 1 | IO3_Output_Tri_En 1: disable 0: enable |
| 26 | R/W | 1 | IO2_Output_Tri_En 1: disable 0: enable |
| 25 | R/W | 1 | IO1_Output_Tri_En 1: disable 0: enable |
| 24 | R/W | 1 | IO0_Output_Tri_En 1: disable 0: enable |
| 23:0 | R/W | 0xFFFFFFFF | Data_Output_Tri_En TCON0 output port D[23:0] output enable, with independent bit control: 1s: disable 0s: enable |

7.2.5.21. TCON_ECC_FIFO_REG (Default Value: 0x00000000)

| Offset: 0x0F8 | | | Register Name: TCON_ECC_FIFO_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | / | ECC_FIFO_BIST_EN 0: disable 1: enable |
| 30 | R/W | / | ECC_FIFO_ERR_FLAG |
| 29:24 | / | / | / |
| 23:16 | R/W | / | ECC_FIFO_ERR_BITS |
| 15:9 | / | / | / |
| 8 | R/W | 0 | ECC_FIFO_BLANK_EN 0: disable ecc function in blanking 1: enable ecc function in blanking ECC function is tent to triggered in blanking area at hv mode, set '0' when in hv mode |
| 7:0 | R/W | / | ECC_FIFO_SETTING Note: bit3 0 enable, 1 disable |

7.2.5.22. TCON_DEBUG_REG (Default Value: 0x00000000)

| Offset: 0x0FC | | | Register Name: TCON_DEBUG_REG |
|---------------|--|--|-------------------------------|
|---------------|--|--|-------------------------------|

| Bit | R/W | Default/Hex | Description |
|-------|-----|-------------|---|
| 31 | R/W | / | TCON0_FIFO_Under_Flow |
| 30 | / | / | / |
| 29 | R | / | TCON0_Field_Polarity 0: second field 1: first field |
| 28 | / | / | / |
| 27:16 | R | / | TCON0_Current_Line |
| 15:14 | / | / | / |
| 13 | R/W | 0 | ECC_FIFO_Bypass 0: used 1: bypass |
| 12:0 | / | / | / |

7.2.5.23. TCON_CEU_CTL_REG (Default Value: 0x00000000)

| Offset: 0x100 | | | Register Name: TCON_CEU_CTL_REG |
|---------------|-----|-------------|----------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | CEU_en 0: bypass 1: enable |
| 30:0 | / | / | / |

7.2.5.24. TCON_CEU_COEF_MUL_REG (Default Value: 0x00000000)

| Offset: 0x110+N*0x04 (N=0,1,2,4,5,6,8,9,10) | | | Register Name: TCON_CEU_COEF_MUL_REG |
|--|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:13 | / | / | / |
| 12:0 | R/W | 0 | CEU_Coef_Mul_Value signed 13bit value, range of (-16,16) N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb |

7.2.5.25. TCON_CEU_COEF_ADD_REG (Default Value: 0x00000000)

| Offset: 0x11C+N*0x10 (N=0,1,2) | | | Register Name: TCON_CEU_COEF_ADD_REG |
|-----------------------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:19 | / | / | / |
| 18:0 | R/W | 0 | CEU_Coef_Add_Value signed 19bit value, range of (-16384, 16384) |

| | | | |
|--|--|--|-------------------------------|
| | | | N=0: Rc N=1: Gc N=2: Bc |
|--|--|--|-------------------------------|

7.2.5.26. TCON_CEU_COEF_RANG_REG (Default Value: 0x00000000)

| Offset: 0x140+N*0x04 (N=0,1,2) | | | Register Name: TCON_CEU_COEF_RANG_REG |
|-----------------------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:16 | R/W | 0 | CEU_Coef_Range_Min unsigned 8bit value, range of [0,255] |
| 15:8 | / | / | / |
| 7:0 | R/W | 0 | CEU_Coef_Range_Max unsigned 8bit value, range of [0,255] |

7.2.5.27. TCON0_CPU_TRI0_REG (Default Value: 0x00000000)

| Offset: 0x160 | | | Register Name: TCON0_CPU_TRI0_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:28 | / | / | / |
| 27:16 | R/W | 0 | Block_Space should be set >20*pixel_cycle |
| 15:12 | / | / | / |
| 11:0 | R/W | 0 | Block_Size |

7.2.5.28. TCON0_CPU_TRI1_REG (Default Value: 0x00000000)

| Offset: 0x164 | | | Register Name: TCON0_CPU_TRI1_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:16 | R | 0 | Block_Current_Num |
| 15:0 | R/W | 0 | Block_Num |

7.2.5.29. TCON0_CPU_TRI2_REG (Default Value: 0x00200000)

| Offset: 0x168 | | | Register Name: TCON0_CPU_TRI2_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | R/W | 0x20 | Start_Delay Tdly = (Start_Delay +1) * be_clk*8 |
| 15 | R/W | 0 | Trans_Start_Mode 0: ecc_fifo+tri_fifo 1: tri_fifo |
| 14:13 | R/W | 0 | Sync_Mode 0x: auto 10: 0 11: 1 |
| 12:0 | R/W | 0 | Trans_Start_Set |

7.2.5.30. TCON0_CPU_TRI3_REG (Default Value: 0x00000000)

| Offset: 0x16C | | | Register Name: TCON0_CPU_TRI3_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:30 | / | / | / |
| 29:28 | R/W | 0 | Tri_Int_Mode 00: disable 01: counter mode 10: te rising mode 11: te falling mode when set as 01, Tri_Counter_Int occur in cycle of (Count_N+1)×(Count_M+1)×4 dclk. when set as 10 or 11, io0 is map as TE input. |
| 27:24 | / | / | / |
| 23:8 | R/W | 0 | Counter_N |
| 7:0 | R/W | 0 | Counter_M |

7.2.5.31. TCON_CMAP_CTL_REG (Default Value: 0x00000000)

| Offset: 0x180 | | | Register Name: TCON_CMAP_CTL_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | Color_Map_En 0: bypass 1: enable This module only work when X is divided by 4 |
| 30:1 | / | / | / |
| 0 | R/W | 0 | Out_Format 0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3 1: 2 pixel output mode: Out0 -> Out1 |

7.2.5.32. TCON_CMAP_ODD0_REG (Default Value: 0x00000000)

| Offset: 0x190 | | | Register Name: TCON_CMAP_ODD0_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | R/W | 0 | Out_Odd1 |
| 15:0 | R/W | 0 | Out_Odd0 bit15-12: Reservd bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0x0: in_b0 0x1: in_g0 0x2: in_r0 0x3: reservd 0x4: in_b1 0x5: in_g1 0x6: in_r1 0x7: reservd |

| | | | |
|--|--|--|--|
| | | | 0x8: in_b2 0x9: in_g2 0xa: in_r2 0xb: reservd 0xc: in_b3 0xd: in_g3 0xe: in_r3 0xf: reservd |
|--|--|--|--|

7.2.5.33. TCON_CMAP_ODD1_REG (Default Value: 0x00000000)

| Offset: 0x194 | | | Register Name: TCON_CMAP_ODD1_REG |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:16 | R/W | 0 | Out_Odd3 |
| 15:0 | R/W | 0 | Out_Odd2 |

7.2.5.34. TCON_CMAP_EVEN0_REG (Default Value: 0x00000000)

| Offset: 0x198 | | | Register Name: TCON_CMAP_EVEN0_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | R/W | 0 | Out_Even1 |
| 15:0 | R/W | 0 | Out_Even0 |

7.2.5.35. TCON_CMAP_EVEN1_REG (Default Value: 0x00000000)

| Offset: 0x19C | | | Register Name: TCON_CMAP_EVEN1_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | R/W | 0 | Out_Even3 |
| 15:0 | R/W | 0 | Out_Even2 |

7.2.5.36. TCON_SAFE_PERIOD_REG (Default Value: 0x00000000)

| Offset: 0x1F0 | | | Register Name: TCON_SAFE_PERIOD_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28:16 | R/W | 0 | Safe_Period_FIFO_Num |
| 15:2 | / | / | / |
| 1:0 | R/W | 0 | Safe_Period_Mode 0: unsafe 1: safe 2: safe at ecc_fifo_curr_num > safe_period_fifo_num 3: safe at 2 and safe at sync active |

7.2.5.37. TCON0_LVDS_ANA0_REG (Default Value: 0x00000000)

| Offset: 0x220 | | | Register Name: TCON_LVDS_ANA0_REG |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | lvds0_en_mb enable the bias circuit of the LVDS_Ana module |
| 30 | R/W | 0 | lvds0_en_ldo |
| 29:25 | / | / | / |
| 24 | R/W | 0 | lvds0_en_drvc enable all circuits working when transmitting the data in channel clock of LVDS_tx0 |
| 23:20 | R/W | 0 | lvds0_en_drv enable all circuits working when transmitting the data in channel<3:0> of LVDS_tx0 |
| 19 | / | / | / |
| 18:17 | R/W | 0 | lvds0_reg_c adjust current flowing through Rload of Rx to change the differential signals amplitude 0:250mV 1:300mV 2:350mV 3:400mV |
| 16 | R/W | 0 | lvds0_reg_denc choose data output or PLL test clock output in LVDS_tx |
| 15:12 | R/W | 0 | lvds0_reg_den choose data output or PLL test clock output in LVDS_tx |
| 11:10 | / | / | / |
| 9:8 | R/W | 0 | lvds0_reg_v adjust common mode voltage of the differential signals in five channels single signal high level: 0:1.1V 1:1.19V 2:1.3V 3:1.43V |
| 7:6 | / | / | / |
| 5:4 | R/W | 0 | lvds0_reg_pd fine adjust the slew rate of output data |
| 3:2 | / | / | / |
| 1 | R/W | 0 | lvds0_reg_pwslv adjust voltage amplitude of low power in LVDS_Ana |
| 0 | R/W | 0 | lvds0_reg_pwsmb adjust voltage amplitude of mbias voltage reference in LVDS_Ana |

Chapter 8 Interfaces

This chapter describes the S3 interfaces, including:

- TWI
- SPI
- UART
- USB
- I2S/PCM
- EMAC

Sochip

8.1. TWI

8.1.1. Overview

This TWI controller is designed to be used as an interface between CPU host and the serial TWI bus. It can support all the standard TWI transfer, including slave and master. The communication to the TWI bus is carried out on a byte-wise basis using interrupt or polled handshaking. This TWI controller can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple masters and 10-bit addressing mode are supported for this specified application. General call addressing is also supported in slave mode.

The TWI Controller includes the following features:

- Software-programmable for slave or master
- Support Repeated START signal
- Multi-master systems supported
- Allow 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and general call address detection
- Interrupt on address detection
- Support speeds up to 400Kbits/s ("fast mode")
- Allow operation from a wide range of input clock frequency

8.1.2. Timing Diagram

Data transferred are always in a unit of 8-bit (byte), followed by an acknowledge bit. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred in serial with the MSB first. Between each byte of data transfer, a receiver device will hold the clock line SCL low to force the transmitter into a wait state while waiting the response from microprocessor.

Data transfer with acknowledge is obligatory. The clock line is driven by the master all the time, including the acknowledge-related clock cycle, except for the SCL holding between each bytes. After sending each byte, the transmitter releases the SDA line to allow the receiver to pull down the SDA line and send an acknowledge signal (or leave it high to send a "not acknowledge") to the transmitter.

When a slave receiver doesn't acknowledge the slave address (unable to receive because of no resource available), the data line must be left high by the slave so that the master can then generate a STOP condition to abort the transfer. Slave receiver can also indicate not to want to send more data during a transfer by leave the acknowledge signal high. And the master should generate the STOP condition to abort the transfer.

Below diagram provides an illustration the relation of SDA signal line and SCL signal line on the TWI serial bus.

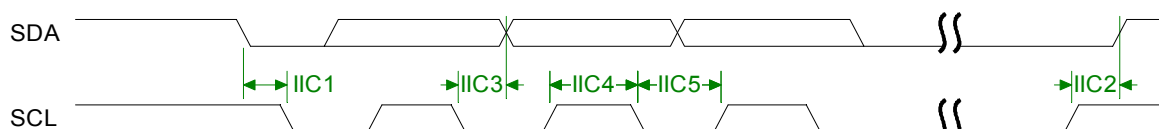


Figure 8-1 . TWI Timing Diagram

8.1.3. TWI Controller Special Requirement

8.1.3.1. TWI Pin List

| Port Name | Direction | Description |
|-----------|-----------|----------------------|
| TWI_SCL | IN/OUT | TWI Clock line |
| TWI_SDA | IN/OUT | TWI Serial Data line |

8.1.3.2. TWI Controller Operation

There are four operation modes on the TWI bus which dictates the communications method. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing commands and data to its registers. The TWI interrupts the CPU host for the attention each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit in the 2WIRE_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit high.

In Slave Mode, the TWI also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

8.1.4. TWI Controller Register List

| Module Name | Base Address |
|-------------|--------------|
| TWI0 | 0x01C2AC00 |
| TWI1 | 0x01C2B000 |

| Register Name | Offset | Description |
|---------------|--------|------------------------------|
| TWI_ADDR | 0x0000 | TWI Slave address |
| TWI_XADDR | 0x0004 | TWI Extended slave address |
| TWI_DATA | 0x0008 | TWI Data byte |
| TWI_CNTR | 0x000C | TWI Control register |
| TWI_STAT | 0x0010 | TWI Status register |
| TWI_CCR | 0x0014 | TWI Clock control register |
| TWI_SRST | 0x0018 | TWI Software reset |
| TWI_EFR | 0x001C | TWI Enhance Feature register |
| TWI_LCR | 0x0020 | TWI Line Control register |

8.1.5. TWI Controller Register Description

8.1.5.1. TWI Slave Address Register(Default Value: 0x00000000)

| Offset: 0x00 | | | Register Name: TWI_ADDR |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:1 | R/W | 0 | SLA Slave address <ul style="list-style-type: none"> • 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 • 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8] |
| 0 | R/W | 0 | GCE General call address enable 0: Disable 1: Enable |

Notes:

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

8.1.5.2. TWI Extend Address Register(Default Value: 0x00000000)

| Offset: 0x04 | | | Register Name: TWI_XADDR |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:0 | R/W | 0 | SLAX Extend Slave Address SLAX[7:0] |

8.1.5.3. TWI Data Register(Default Value: 0x00000000)

| Offset: 0x08 | | | Register Name: TWI_DATA |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:0 | R/W | 0 | TWI_DATA Data byte for transmitting or received |

8.1.5.4. TWI Control Register(Default Value: 0x00000000)

| Offset: 0x0C | | | Register Name: TWI_CNTR |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R/W | 0 | INT_EN Interrupt Enable 1'b0: The interrupt line always low 1'b1: The interrupt line will go high when INT_FLAG is set. |
| 6 | R/W | 0 | BUS_EN TWI Bus Enable 1'b0: The TWI bus inputs ISDA/ISCL are ignored and the TWI Controller will not respond to any address on the bus 1'b1: The TWI will respond to calls to its slave address – and to the general call address if the GCE bit in the ADDR register is set. Notes: In master operation mode, this bit should be set to '1' |
| 5 | R/W | 0 | M_STA Master Mode Start When M_STA is set to '1', TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent: writing a '0' to this bit has no effect. |
| 4 | R/W | 0 | M_STP Master Mode Stop If M_STP is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a '0' to this bit has no effect. |
| 3 | R/W | 0 | INT_FLAG Interrupt Flag INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low. |
| 2 | R/W | 0 | A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: <ol style="list-style-type: none"> 1. Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. 2. The general call address has been received and the GCE bit in the ADDR register is set to '1'. 3. A data byte has been received in master or slave mode. |

| | | | |
|-----|-----|---|---|
| | | | When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set. |
| 1:0 | R/W | 0 | / |

8.1.5.5. TWI Status Register(Default Value: 0x000000F8)

| Offset: 0x10 | | | Register Name: TWI_STAT |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:0 | R | 0xF8 | STA Status Information Byte Code Status 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved |

8.1.5.6. TWI Clock Register(Default Value: 0x00000000)

| Offset: 0x14 | | | Register Name: TWI_CCR |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:7 | / | / | / |
| 6:3 | R/W | 0 | CLK_M |
| 2:0 | R/W | 0 | CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: $F_{\text{samp}} = F_0 = F_{\text{in}} / 2^{\text{CLK_N}}$ The TWI OSCL output frequency, in master mode, is F1 / 10: $F_1 = F_0 / (\text{CLK_M} + 1)$ $F_{\text{oscl}} = F_1 / 10 = F_{\text{in}} / (2^{\text{CLK_N}} * (\text{CLK_M} + 1) * 10)$ For Example: Fin = 48Mhz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 2, CLK_M=2 $F_0 = 48\text{M} / 2^2 = 12\text{Mhz}$, $F_1 = F_0 / (10 * (2+1)) = 0.4\text{Mhz}$ For 100Khz standard speed 2Wire, CLK_N=2, CLK_M=11 $F_0 = 48\text{M} / 2^2 = 12\text{Mhz}$, $F_1 = F_0 / (10 * (11+1)) = 0.1\text{Mhz}$ |

8.1.5.7. TWI Soft Reset Register(Default Value: 0x00000000)

| Offset: 0x18 | | | Register Name: TWI_SRST |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:1 | / | / | / |
| 0 | R/W | 0 | SOFT_RST Soft Reset Write '1' to this bit to reset the TWI and clear to '0' when completing Soft Reset operation. |

8.1.5.8. TWI Enhance Feature Register(Default Value: 0x00000000)

| Offset: 0x1C | | | Register Name: TWI_EFR |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:2 | / | / | / |
| 0:1 | R/W | 0 | DBN Data Byte number follow Read Command Control 0— No Data Byte to be written after read command 1— Only 1 byte data to be written after read command 2— 2 bytes data can be written after read command 3— 3 bytes data can be written after read command |

8.1.5.9. TWI Line Control Register(Default Value: 0x0000003A)

| Offset: 0x20 | | | Register Name: TWI_LCR |
|--------------|-----|-------------|-------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:6 | / | / | / |
| 5 | R | 1 | SCL_STATE |

| | | | |
|---|-----|---|---|
| | | | Current state of TWI_SCL 0 - low 1 - high |
| 4 | R | 1 | SDA_STATE Current state of TWI_SDA 0 - low 1 - high |
| 3 | R/W | 1 | SCL_CTL TWI_SCL line state control bit When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL 0 – output low level 1 – output high level |
| 2 | R/W | 0 | SCL_CTL_EN TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is control by the value of bit[3]. 0-disable TWI_SCL line control mode 1-enable TWI_SCL line control mode |
| 1 | R/W | 1 | SDA_CTL TWI_SDA line state control bit When line control mode is enabled (bit[0] set), value of this bit decide the output level of TWI_SDA 0 – output low level 1 – output high level |
| 0 | R/W | 0 | SDA_CTL_EN TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is control by the value of bit[1]. 0-disable TWI_SDA line control mode 1-enable TWI_SDA line control mode |

8.1.5.10. TWI DVFS Control Register(Default Value: 0x00000000)

| Offset: 0x24 | | | Register Name: TWI_DVFSCR |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:3 | / | / | / |
| 2 | R/W | 0 | MS_PRIORITY CPU and DVFS BUSY set priority select 0: CPU has higher priority 1: DVFS has higher priority |
| 1 | R/W | 0 | CPU_BUSY_SET CPU Busy set |
| 0 | R/W | 0 | DVFC_BUSY_SET DVFS Busy set |

Notes: This register is only implemented in TWI0.

8.2. SPI

8.2.1. Overview

The SPI is the Serial Peripheral Interface which allows rapid data communication with fewer software interrupts. It can interface with up to four slave external devices or one single external master. The SPI module contains one 64x8 receiver buffer (RXFIFO) and one 64x8 transmit buffer (TXFIFO). It can work at two modes: Master mode and Slave mode.

The SPI includes the following features:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Programmable clock granularity
- Up to four chip selects to support multiple peripherals
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) are configurable

8.2.2. SPI Timing Diagram

The serial peripheral interface master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

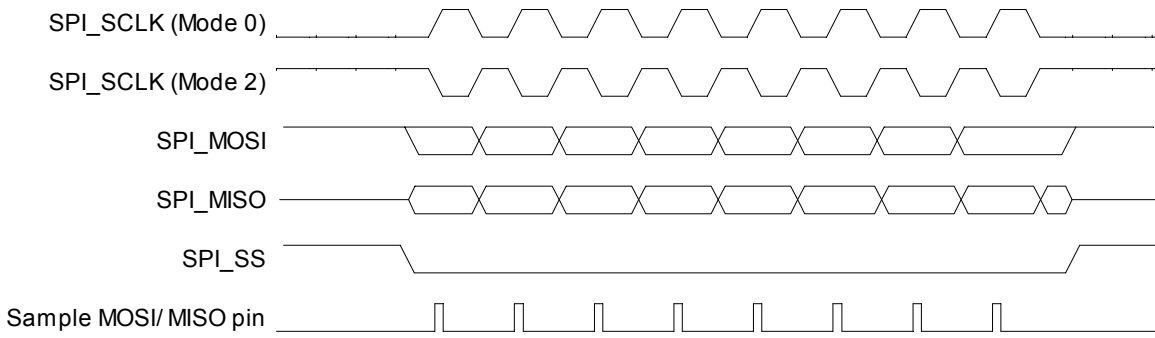
During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four kinds of modes are listed below:

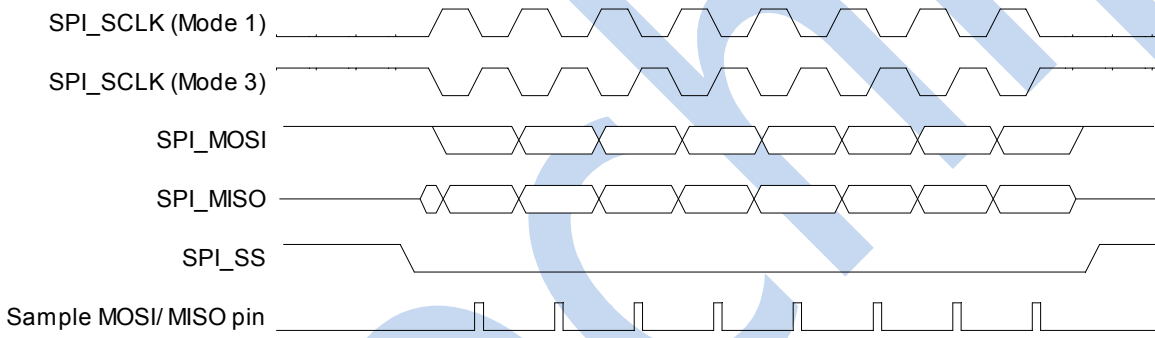
Table 8-1. Four mode of SPI

| SPI Mode | POL | PHA | Leading Edge | Trailing Edge |
|----------|-----|-----|-----------------|-----------------|
| 0 | 0 | 0 | Rising, Sample | Falling, Setup |
| 1 | 0 | 1 | Rising, Setup | Falling, Sample |
| 2 | 1 | 0 | Falling, Sample | Rising, Setup |
| 3 | 1 | 1 | Falling, Setup | Rising, Sample |



Phase 0

Figure 8-2 . SPI Phase 0 Timing Diagram



Phase 1

Figure 8-3. SPI Phase 1 Timing Diagram

8.2.3. SPI Special Requirement

8.2.3.1. SPI Pin List

The direction of SPI pin is different in two work modes: Master Mode and Slave Mode.

Table 8-2. SPI Pin Description

| Port Name | Width | Direction(M) | Direction(S) | Description |
|-------------|-------|--------------|--------------|---|
| SPI_SCLK | 1 | OUT | IN | SPI Clock |
| SPI_MOSI | 1 | OUT | IN | SPI Master Output Slave Input Data Signal |
| SPI_MISO | 1 | IN | OUT | SPI Master Input Slave Output Data Signal |
| SPI_SS[3:0] | 4 | OUT | IN | SPI Chip Select Signal |

8.2.3.2. SPI Module Clock Source and Frequency

The SPI Controller get three different clocks, users can select one of them to make SPI Clock Source. The SPI_SCLK can in the range from 3KHz to 100 MHz. The following table describes the clock sources for SPI Controller. Users can see **Clock Controller Uint(CCU)** in chapter 4 for clock setting, configuration and gating information.

Table 8-3. SPI Clock Sources

| Clock Name | Description |
|-------------|---|
| OSC24M | 24MHz Crystal |
| PLL_PERIPH0 | Peripheral Clock, default value is 600MHz |
| PLL_PERIPH1 | Peripheral Clock, default value is 600MHz |

8.2.4. SPI Register List

| Module Name | Base Address |
|-------------|--------------|
| SPI | 0x01C68000 |

| Register Name | Offset | Description |
|---------------|--------|---------------------------------|
| SPI_GCR | 0x04 | SPI Global Control Register |
| SPI_TCR | 0x08 | SPI Transfer Control register |
| / | 0x0c | reserved |
| SPI_IER | 0x10 | SPI Interrupt Control register |
| SPI_ISR | 0x14 | SPI Interrupt Status register |
| SPI_FCR | 0x18 | SPI FIFO Control register |
| SPI_FSR | 0x1C | SPI FIFO Status register |
| SPI_WCR | 0x20 | SPI Wait Clock Counter register |
| SPI_CCR | 0x24 | SPI Clock Rate Control register |
| / | 0x28 | reserved |
| / | 0x2c | reserved |
| SPI_MBC | 0x30 | SPI Burst Counter register |
| SPI_MTC | 0x34 | SPI Transmit Counter Register |
| SPI_BCC | 0x38 | SPI Burst Control register |
| SPI_TXD | 0x200 | SPI TX Data register |
| SPI_RXD | 0x300 | SPI RX Data register |

8.2.5. SPI Register Description

8.2.5.1. SPI Global Control Register(Default Value: 0x00000080)

| Offset: 0x04 | | | Register Name: SPI_CTL |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | SRST Soft reset Write '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes Write '0' has no effect. |
| 30:8 | / | / | / |
| 7 | R/W | 1 | TP_EN |

| | | | |
|-----|-----|---|--|
| | | | <p>Transmit Pause Enable</p> <p>In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full.</p> <p>1 – stop transmit data when RXFIFO full</p> <p>0 – normal operation, ignore RXFIFO status</p> <p>Note: Can't be written when XCH=1</p> |
| 6:2 | / | / | / |
| 1 | R/W | 0 | <p>MODE</p> <p>SPI Function Mode Select</p> <p>0: Slave Mode</p> <p>1: Master Mode</p> <p>Note: Can't be written when XCH=1</p> |
| 0 | R/W | 0 | <p>EN</p> <p>SPI Module Enable Control</p> <p>0: Disable</p> <p>1: Enable</p> |

8.2.5.2. SPI Transfer Control Register(Default Value: 0x00000087)

| Offset: 0x08 | | | Register Name: SPI_INTCTL |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0x0 | <p>XCH</p> <p>Exchange Burst</p> <p>In master mode it is used to start SPI burst</p> <p>0: Idle</p> <p>1: Initiates exchange.</p> <p>Write "1" to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Write "1" to SRST will also clear this bit. Write '0' to this bit has no effect.</p> <p>Note: Can't be written when XCH=1.</p> |
| 30:14 | / | / | / |
| 13 | R/W | 0x0 | <p>SDM</p> <p>Master Sample Data Mode</p> <p>0 - Delay Sample Mode</p> <p>1 - Normal Sample Mode</p> <p>In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode;</p> <p>In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.</p> |
| 12 | R/W | 0x0 | <p>FBS</p> <p>First Transmit Bit Select</p> <p>0: MSB first</p> <p>1: LSB first</p> <p>Note: Can't be written when XCH=1.</p> |
| 11 | R/W | 0x0 | <p>SDC</p> <p>Master Sample Data Control</p> <p>Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave.</p> <p>0: normal operation, do not delay internal read sample point</p> <p>1: delay internal read sample point</p> <p>Note: Can't be written when XCH=1.</p> |

| | | | |
|-----|-----|-----|---|
| 10 | R/W | 0x0 | <p>RPSM Rapids mode select Select Rapids mode for high speed write. 0: normal write mode 1: rapids write mode Note: Can't be written when XCH=1.</p> |
| 9 | R/W | 0x0 | <p>DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Note: Can't be written when XCH=1.</p> |
| 8 | R/W | 0x0 | <p>DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. Note: Can't be written when XCH=1.</p> |
| 7 | R/W | 0x1 | <p>SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high Note: Can't be written when XCH=1.</p> |
| 6 | R/W | 0x0 | <p>SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software Note: Can't be written when XCH=1.</p> |
| 5:4 | R/W | 0x0 | <p>SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Note: Can't be written when XCH=1.</p> |
| 3 | R/W | 0x0 | <p>SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Note: Can't be written when XCH=1.</p> |
| 2 | R/W | 0x1 | <p>SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Note: Can't be written when XCH=1.</p> |
| 1 | R/W | 0x1 | <p>CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle)</p> |

| | | | |
|---|-----|-----|---|
| | | | 1: Active low polarity (1 = Idle) Note: Can't be written when XCH=1. |
| 0 | R/W | 0x1 | CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Note: Can't be written when XCH=1. |

8.2.5.3. SPI Interrupt Control Register(Default Value: 0x00000000)

| Offset: 0x10 | | | Register Name: SPI_IER |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | R | 0x0 | Reserved. |
| 13 | R/W | 0x0 | SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable |
| 12 | R/W | 0x0 | TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable |
| 11 | R/W | 0x0 | TF_UDR_INT_EN TXFIFO under run Interrupt Enable 0: Disable 1: Enable |
| 10 | R/W | 0x0 | TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable |
| 9 | R/W | 0x0 | RF_UDR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable |
| 8 | R/W | 0x0 | RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable |
| 7 | R | 0x0 | Reserved. |
| 6 | R/W | 0x0 | TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable |
| 5 | R/W | 0x0 | TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable |
| 4 | R/W | 0x0 | TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable |
| 3 | R | 0x0 | Reserved |

| | | | |
|---|-----|-----|--|
| 2 | R/W | 0x0 | RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable |
| 1 | R/W | 0x0 | RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable |
| 0 | R/W | 0x0 | RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable |

8.2.5.4. SPI Interrupt Status Register(Default Value: 0x00000022)

| Offset: 0x14 | | | Register Name: SPI_INT_STA |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | 0x0 | / |
| 13 | R/W | 0 | SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it. |
| 12 | R/W | 0 | TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed |
| 11 | R/W | 0 | TF_UDF TXFIFO Underrun This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun |
| 10 | R/W | 0 | TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed |
| 9 | R/W | 0 | RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it. |
| 8 | R/W | 0 | RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed. |
| 7 | / | / | / |
| 6 | R/W | 0 | TX_FULL TXFIFO Full |

| | | | |
|---|-----|---|--|
| | | | This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full |
| 5 | R/W | 1 | TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty |
| 4 | R/W | 0 | TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing "1" to this bit clears it. Where TX_WL is the water level of RXFIFO |
| 3 | / | / | reserved |
| 2 | R/W | 0 | RX_FULL RXFIFO Full This bit is set when the RXFIFO is full . Writing 1 to this bit clears it. 0: Not Full 1: Full |
| 1 | R/W | 1 | RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty . Writing 1 to this bit clears it. 0: Not empty 1: empty |
| 0 | R/W | 0 | RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing "1" to this bit clears it. Where RX_WL is the water level of RXFIFO. |

8.2.5.5. SPI FIFO Control Register(Default Value: 0x00400001)

| Offset: 0x18 | | | Register Name: SPI_FCR |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | TX_FIFO_RST TX FIFO Reset Write '1' to this bit will reset the control portion of the TX FIFO and auto clear to '0' when completing reset operation, write to '0' has no effect. |
| 30 | R/W | 0 | TF_TEST_ENB TX Test Mode Enable 0: disable 1: enable Note: In normal mode, TX FIFO can only be read by SPI controller, write '1' to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time. |
| 29:26 | / | / | / |
| 25 | / | / | / |
| 24 | R/W | 0x0 | TF_DRQ_EN TX FIFO DMA Request Enable |

| | | | |
|-------|-----|------|---|
| | | | 0: Disable 1: Enable |
| 23:16 | R/W | 0x40 | TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level |
| 15 | R/W | 0x0 | RF_RST RXFIFO Reset Write '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, write '0' to this bit has no effect. |
| 14 | R/W | 0x0 | RF_TEST RX Test Mode Enable 0: Disable 1: Enable Note: In normal mode, RX FIFO can only be written by SPI controller, write '1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time. |
| 13:10 | R | 0x0 | Reserved |
| 9 | R/W | 0x0 | RX_DMA_MODE SPI RX DMA Mode Control 0: Normal DMA mode 1: Dedicate DMA mode |
| 8 | R/W | 0x0 | RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable |
| 7:0 | R/W | 0x1 | RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level |

8.2.5.6. SPI FIFO Status Register(Default Value: 0x00000000)

| Offset: 0x1C | | | Register Name: SPI_FSR |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R | 0x0 | TB_WR TX FIFO Write Buffer Write Enable |
| 30:28 | R | 0x0 | TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer |
| 27:24 | R | 0x0 | Reserved |
| 23:16 | R | 0x0 | TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO ... 64: 64 bytes in TX FIFO |
| 15 | R | 0x0 | RB_WR RX FIFO Read Buffer Write Enable |
| 14:12 | R | 0x0 | RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer |
| 11:8 | R | 0x0 | Reserved |

| | | | |
|-----|---|-----|--|
| 7:0 | R | 0x0 | RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO ... 64:64 bytes in RX FIFO |
|-----|---|-----|--|

8.2.5.7. SPI Wait Clock Register(Default Value: 0x0000_0000)

| Offset: 0x20 | | | Register Name: SPI_WAIT |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:20 | / | / | / |
| 19:16 | R/W | 0x0 | SWC Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted n: n SPI_SCLK wait states inserted Note: These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. Note: Can't be written when XCH=1. |
| 15:0 | R/W | 0 | WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted |

8.2.5.8. SPI Clock Control Register(Default Value: 0x00000002)

| Offset: 0x24 | | | Register Name: SPI_CCTL |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:13 | / | / | / |
| 12 | R/W | 0 | DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2 |
| 11:8 | R/W | 0 | CDR1 Clock Divide Rate 1 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / 2^n. |
| 7:0 | R/W | 0x2 | CDR2 Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(n + 1)). |

8.2.5.9. SPI Master Burst Counter Register(Default Value: 0x00000000)

| Offset: 0x30 | | | Register Name: SPI_BC |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:0 | R/W | 0 | MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst ... N: N bursts |

8.2.5.10. SPI Master Transmit Counter Register(Default Value: 0x00000000)

| Offset: 0x34 | | | Register Name: SPI_TC |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23:0 | R/W | 0 | MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst ... N: N bursts |

8.2.5.11. SPI Master Burst Control Counter Register(Default Value: 0x00000000)

| Offset: 0x38 | | | Register Name: SPI_BCC |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | R | 0x0 | Reserved |
| 28 | R/W | 0x0 | DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode Note: Can't be written when XCH=1. |
| 27:24 | R/W | 0x0 | DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don't care by the device. 0: 0 burst 1: 1 burst ... N: N bursts Note: Can't be written when XCH=1. |
| 23:0 | R/W | 0x0 | STC Master Single Mode Transmit Counter |

| | | | |
|--|--|--|--|
| | | | <p>In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts.</p> <p>0: 0 burst 1: 1 burst ... N: N bursts</p> <p>Note: Can't be written when XCH=1.</p> |
|--|--|--|--|

8.2.5.12. SPI TX Data Register(Default Value: 0x00000000)

| Offset: 0x200 | | | Register Name: SPI_TXD |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | W/R | 0x0 | <p>TDATA Transmit Data</p> <p>This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in RXFIFO, one burst data is written to RXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4.</p> <p>Note: This address is writing-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.</p> |

8.2.5.13. SPI RX Data Register(Default Value: 0x00000000)

| Offset: 0x300 | | | Register Name: SPI_RXD |
|---------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | <p>RDATA Receive Data</p> <p>This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4.</p> <p>Note: This address is read-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.</p> |

8.3. UART

8.3.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports data lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

The UART includes the following features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- DMA controller interface
- Software/ Hardware Flow Control
- Programmable Transmit Holding Register Empty interrupt
- Interrupt support for FIFOs, Status Change
- Support IrDA 1.0 SIR

8.3.2. UART Timing Diagram

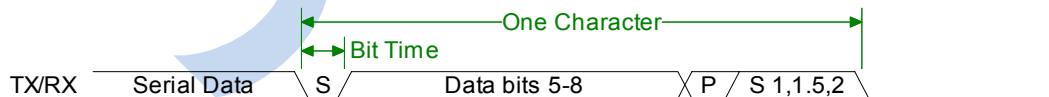


Figure 8-4. UART Serial Data Format

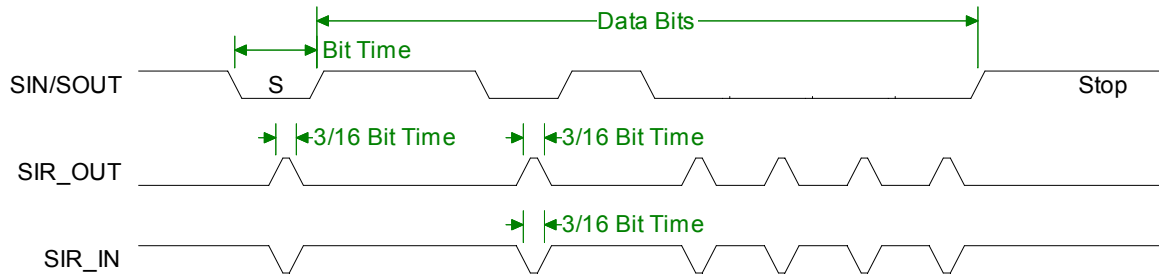


Figure 8-5. Serial IrDA Data Format

8.3.3. UART Pin List

| Port Name | Direction | Description |
|-----------|-----------|---|
| UART0_TX | OUT | UART Serial Bit output |
| UART0_RX | IN | UART Serial Bit input |
| UART1_TX | OUT | UART Serial Bit output |
| UART1_RX | IN | UART Serial Bit input |
| UART1_RTS | OUT | UART Request To Send This active low output signal informs Modem that the UART is ready to send data |
| UART1_CTS | IN | UART Clear To End This active low signal is an input showing when Modem is ready to accept data |
| UART2_TX | OUT | UART Serial Bit output |
| UART2_RX | IN | UART Serial Bit input |
| UART2_RTS | OUT | UART Request To Send This active low output signal informs Modem that the UART is ready to send data |
| UART2_CTS | IN | UART Clear To End This active low signal is an input showing when Modem is ready to accept data |

8.3.4. UART Register List

There are 3 UART controllers. All UART controllers can be configured as Serial IrDA.

| Module Name | Base Address |
|-------------|--------------|
| UART0 | 0x01C28000 |
| UART1 | 0x01C28400 |
| UART2 | 0x01C28800 |

| Register Name | Offset | Description |
|---------------|--------|----------------------------------|
| UART_RBR | 0x00 | UART Receive Buffer Register |
| UART_THR | 0x00 | UART Transmit Holding Register |
| UART_DLL | 0x00 | UART Divisor Latch Low Register |
| UART_DLH | 0x04 | UART Divisor Latch High Register |
| UART_IER | 0x04 | UART Interrupt Enable Register |
| UART_IIR | 0x08 | UART Interrupt Identity Register |
| UART_FCR | 0x08 | UART FIFO Control Register |
| UART_LCR | 0x0C | UART Line Control Register |
| UART_MCR | 0x10 | UART Modem Control Register |

| | | |
|-----------|------|----------------------------|
| UART_LSR | 0x14 | UART Line Status Register |
| UART_MSR | 0x18 | UART Modem Status Register |
| UART_SCH | 0x1C | UART Scratch Register |
| UART_USR | 0x7C | UART Status Register |
| UART_TFL | 0x80 | UART Transmit FIFO Level |
| UART_RFL | 0x84 | UART_RFL |
| UART_HALT | 0xA4 | UART Halt TX Register |

8.3.5. UART Register Description

8.3.5.1. UART Receiver Buffer Register(Default Value: 0x00000000)

| Offset: 0x0000 | | | Register Name: UART_RBR |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:0 | R | 0 | RBR Receiver Buffer Register Data byte received on the serial input port . The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs. |

8.3.5.2. UART Transmit Holding Register(Default Value: 0x00000000)

| Offset: 0x0000 | | | Register Name: UART_THR |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:0 | W | 0 | THR Transmit Holding Register Data to be transmitted on the serial output port . Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost. |

8.3.5.3. UART Divisor Latch Low Register(Default Value: 0x00000000)

| Offset: 0x0000 | | | Register Name: UART_DLL |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:0 | R/W | 0 | DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the |

| | | | |
|--|--|--|---|
| | | | <p>DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.</p> |
|--|--|--|---|

8.3.5.4. UART Divisor Latch High Register(Default Value: 0x00000000)

| Offset: 0x0004 | | | Register Name: UART_DLH |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:0 | R/W | 0 | <p>DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.</p> |

8.3.5.5. UART Interrupt Enable Register(Default Value: 0x00000000)

| Offset: 0x0004 | | | Register Name: UART_IER |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R/W | | <p>PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable</p> |
| 6:4 | / | / | / |
| 3 | R/W | 0 | <p>EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable</p> |
| 2 | R/W | 0 | <p>ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable</p> |
| 1 | R/W | 0 | ETBEI |

| | | | |
|---|-----|---|--|
| | | | <p>Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable</p> |
| 0 | R/W | 0 | <p>ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable</p> |

8.3.5.6. UART Interrupt Identity Register(Default Value: 0x00000000)

| Offset: 0x0008 | | | Register Name: UART_IIR |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:6 | R | 0 | <p>FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable</p> |
| 5:4 | / | / | / |
| 3:0 | R | 0x1 | <p>IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.</p> |

| Interrupt ID | Priority Level | Interrupt Type | Interrupt Source | Interrupt Reset |
|--------------|----------------|------------------------------|--|--|
| 0001 | - | None | None | - |
| 0110 | Highest | Receiver line status | Overflow/parity/ framing errors or break interrupt | Reading the line status register |
| 0100 | Second | Received data available | Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled) | Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled) |
| 1100 | Second | Character timeout indication | No characters in or out of the RCVR FIFO during the last 4 character times and there is at | Reading the receiver buffer register |

| | | | | |
|------|--------|---------------------------------|--|--|
| | | | least 1character in it during This time | |
| 0010 | Third | Transmit holding register empty | Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled) | Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled). |
| 0000 | Fourth | Modem status | Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt. | Reading the Modem status Register |
| 0111 | Fifth | Busy detect indication | UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one). | Reading the UART status register |

8.3.5.7. UART FIFO Control Register(Default Value: 0x00000000)

| Offset: 0x0008 | | | Register Name: UART_FCR |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:6 | W | 0 | RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full |
| 5:4 | W | 0 | TFT TX Empty Trigger Writes have no effect when THRE_MODE_USER = Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full |
| 3 | W | 0 | DMAM DMA Mode 0: Mode 0 1: Mode 1 |
| 2 | W | 0 | XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. |

| | | | |
|---|---|---|--|
| | | | It is 'self-clearing'. It is not necessary to clear this bit. |
| 1 | W | 0 | <p>RFIFOR RCVR FIFO Reset</p> <p>This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request.</p> <p>It is 'self-clearing'. It is not necessary to clear this bit.</p> |
| 0 | W | 0 | <p>FIFOE Enable FIFOs</p> <p>This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.</p> |

8.3.5.8. UART Line Control Register(Default Value: 0x00000000)

| Offset: 0x000C | | | Register Name: UART_LCR |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R/W | 0 | <p>DLAB Divisor Latch Access Bit</p> <p>It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.</p> <p>0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)</p> |
| 6 | R/W | 0 | <p>BC Break Control Bit</p> <p>This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.</p> |
| 5:4 | R/W | 0 | <p>EPS Even Parity Select</p> <p>It is writeable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is to reverse the LCR[4].</p> <p>00: Odd Parity 01: Even Parity 1X: Reverse LCR[4]</p> |
| 3 | R/W | 0 | <p>PEN Parity Enable</p> <p>It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.</p> <p>0: parity disabled 1: parity enabled</p> |
| 2 | R/W | 0 | <p>STOP Number of stop bits</p> |

| | | | |
|-----|-----|---|---|
| | | | <p>It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit.</p> <p>0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit</p> |
| 1:0 | R/W | 0 | <p>DLS Data Length Select</p> <p>It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows:</p> <p>00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits</p> |

8.3.5.9. UART Modem Control Register(Default Value: 0x00000000)

| Offset: 0x0010 | | | Register Name: UART_MCR |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:7 | / | / | / |
| 6 | R/W | 0 | <p>SIRE SIR Mode Enable 0:IrDA SIR Mode disabled 1:IrDA SIR Mode enabled</p> |
| 5 | R/W | 0 | <p>AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled</p> |
| 4 | R/W | 0 | <p>LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.</p> |
| 3:2 | / | / | / |
| 1 | R/W | 0 | <p>RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The</p> |

| | | | |
|---|-----|---|---|
| | | | <p>Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low.</p> <p>0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0)</p> <p>Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.</p> |
| 0 | R/W | 0 | <p>DTR Data Terminal Ready</p> <p>This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n.</p> <p>0: dtr_n de-asserted (logic 1) 1: dtr_n asserted (logic 0)</p> <p>The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications.</p> <p>Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.</p> |

8.3.5.10. UART Line Status Register(Default Value: 0x00000060)

| Offset: 0x0014 | | | Register Name: UART_LSR |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R | 0 | <p>FIFOERR RX Data Error in FIFO</p> <p>When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.</p> |
| 6 | R | 1 | <p>TEMT Transmitter Empty</p> <p>If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.</p> |
| 5 | R | 1 | <p>THRE TX Holding Register Empty</p> <p>If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register.</p> <p>If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.</p> |
| 4 | R | 0 | <p>BI Break Interrupt</p> <p>This is used to indicate the detection of a break sequence on the serial input</p> |

| | | | |
|---|---|---|--|
| | | | <p>data.</p> <p>It is set whenever the serial input, <i>sin</i>, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits.</p> <p>In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.</p> |
| 3 | R | 0 | <p>FE Framing Error</p> <p>This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data.</p> <p>In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]).</p> <p>0: no framing error 1: framing error</p> <p>Reading the LSR clears the FE bit.</p> |
| 2 | R | 0 | <p>PE Parity Error</p> <p>This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]).</p> <p>0: no parity error 1: parity error</p> <p>Reading the LSR clears the PE bit.</p> |
| 1 | R | 0 | <p>OE Overrun Error</p> <p>This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost.</p> <p>0: no overrun error 1: overrun error</p> <p>Reading the LSR clears the OE bit.</p> |
| 0 | R | 0 | <p>DR Data Ready</p> <p>This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO.</p> <p>0: no data ready 1: data ready</p> <p>This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.</p> |

8.3.5.11. UART Modem Status Register(Default Value: 0x00000000)

| Offset: 0x0018 | | | Register Name: UART_MSR |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R | 0 | <p>DCD Line State of Data Carrier Detect</p> <p>This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set.</p> <p>0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)</p> |
| 6 | R | 0 | <p>RI Line State of Ring Indicator</p> <p>This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set.</p> <p>0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)</p> |
| 5 | R | 0 | <p>DSR Line State of Data Set Ready</p> <p>This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART.</p> <p>0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0)</p> <p>In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).</p> |
| 4 | R | 0 | <p>CTS Line State of Clear To Send</p> <p>This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART.</p> <p>0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0)</p> <p>In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).</p> |
| 3 | R | 0 | <p>DDCD Delta Data Carrier Detect</p> <p>This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read.</p> <p>0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR</p> <p>Reading the MSR clears the DDCD bit.</p> <p>Note: If the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.</p> |
| 2 | R | 0 | <p>TERI Trailing Edge Ring Indicator</p> <p>This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read.</p> <p>0: no change on ri_n since last read of MSR</p> |

| | | | |
|---|---|---|--|
| | | | 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit. |
| 1 | R | 0 | DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. |
| 0 | R | 0 | DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. |

8.3.5.12. UART Scratch Register(Default Value: 0x00000000)

| Offset: 0x001C | | | Register Name: UART_SCH |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7:0 | R/W | 0 | SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART. |

8.3.5.13. UART Status Register(Default Value: 0x00000006)

| Offset: 0x007C | | | Register Name: UART_USR |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:5 | / | / | / |
| 4 | R | 0 | RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full. |
| 3 | R | 0 | RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty |

| | | | |
|---|---|---|--|
| | | | This bit is cleared when the RX FIFO is empty. |
| 2 | R | 1 | TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty. |
| 1 | R | 1 | TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full. |
| 0 | R | 0 | BUSY UART Busy Bit 0: Idle or inactive 1: Busy |

8.3.5.14. UART Transmit FIFO Level Register(Default Value: 0x00000000)

| Offset: 0x0080 | | | Register Name: UART_TFL |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:7 | / | / | / |
| 6:0 | R | 0 | TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO. |

8.3.5.15. UART Receive FIFO Level Register(Default Value: 0x00000000)

| Offset: 0x0084 | | | Register Name: UART_RFL |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:7 | / | / | / |
| 6:0 | R | 0 | RFL Receive FIFO Level This is indicates the number of data entries in the receive FIFO. |

8.3.5.16. UART Halt TX Register(Default Value: 0x00000000)

| Offset: 0x00A4 | | | Register Name: UART_HALT |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:6 | / | / | / |
| 5 | R/W | 0 | SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0:Not invert receiver signal 1:Invert receiver signal |
| 4 | R/W | 0 | SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0:Not invert transmit pulse 1:Invert transmit pulse |

| | | | |
|---|-----|---|--|
| 3 | / | / | / |
| 2 | R/W | 0 | <p>CHANGE_UPDATE</p> <p>After the user using HALT[1] to change the baudrate or LCR configuration, write 1 to update the configuration and waiting this bit self clear to 0 to finish update process. Write 0 to this bit has no effect.</p> <p>1: Update trigger, Self clear to 0 when finish update.</p> |
| 1 | R/W | 0 | <p>CHCFG_AT_BUSY</p> <p>This is an enable bit for the user to change LCR register configuration (except for the DLAB bit) and baudrate register (DLH and DLL) when the UART is busy (USB[0] is 1).</p> <p>1: Enable change when busy</p> |
| 0 | R/W | 0 | <p>HALT_TX</p> <p>Halt TX</p> <p>This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled.</p> <p>0 : Halt TX disabled</p> <p>1 : Halt TX enabled</p> <p>Note: If FIFOs are not enabled, the setting of the halt TX register has no effect on operation.</p> |

8.4. USB

8.4.1. USB OTG Controller

The USB OTG controller is a Dual-Role Device, which can also be configured as a Host-only or Device-only controller, fully compliant with the USB 2.0 Specification. It can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode. It can support high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode. Standard USB transceiver can be used through its UTMI+PHY Level3 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus. For saving CPU bandwidth, USB-OTG DMA interface can support external DMA controller to take care of the data transfer between the memory and USB-OTG FIFO. The USB-OTG core also supports USB power saving functions.

The USB2.0 OTG controller has following features:

- Support Device or Host operation at a time
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in host mode
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a for host mode
- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in device mode
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used
- Supports bi-directional endpoint0 for Control transfer in device mode
- Supports up to 8 User-Configurable Endpoints for Bulk, Isochronous and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5) in device mode
- Supports up to 4032BytesFIFO for EPs (Excluding EP0) in device mode
- Supports High-Bandwidth Isochronous & Interrupt transfers in device mode
- Automated splitting/combining of packets for Bulk transfers in device mode
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Includes interface to an external Normal DMA controller for every EPs

8.4.1.1. USB OTG Block Diagram

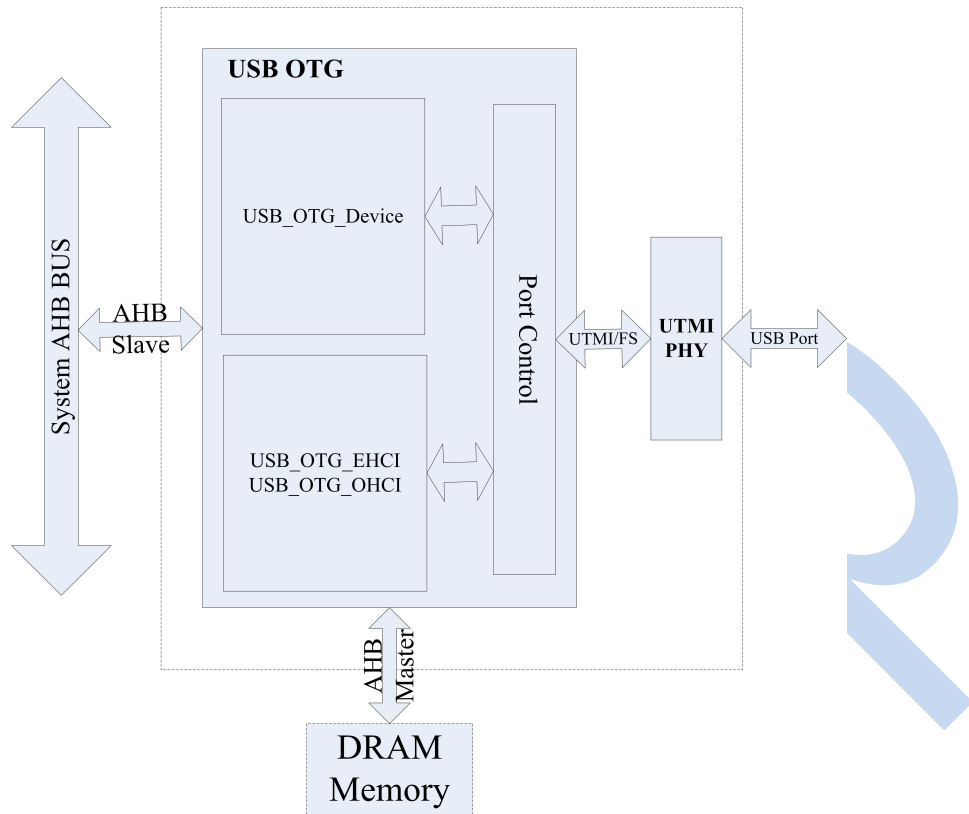


Figure 8-6. USB OTG Controller Block Diagram

8.4.1.2. USB OTG Register List

| Module Name | Base Address |
|-------------|--------------|
| USB_HCI0 | 0x01C1A000 |

| Register Name | Offset | Description |
|----------------------------------|--------|---|
| EHCI Capability Register | | |
| E_CAPLENGTH | 0x000 | EHCI Capability register Length Register |
| E_HCIVERSION | 0x002 | EHCI Host Interface Version Number Register |
| E_HCSPARAMS | 0x004 | EHCI Host Control Structural Parameter Register |
| E_HCCPARAMS | 0x008 | EHCI Host Control Capability Parameter Register |
| E_HCSPPORTROUTE | 0x00c | EHCI Companion Port Route Description |
| EHCI Operational Register | | |
| E_USBCMD | 0x010 | EHCI USB Command Register |
| E_USBSTS | 0x014 | EHCI USB Status Register |
| E_USBINTR | 0x018 | EHCI USB Interrupt Enable Register |
| E_FRINDEX | 0x01c | EHCI USB Frame Index Register |
| E_CTRLDSSEGMENT | 0x020 | EHCI 4G Segment Selector Register |
| E_PERIODICLISTBASE | 0x024 | EHCI Frame List Base Address Register |
| E_ASYNCLISTADDR | 0x028 | EHCI Next Asynchronous List Address Register |
| E_CONFIGFLAG | 0x050 | EHCI Configured Flag Register |

| | | |
|---|-------|-------------------------------------|
| E_PORTSC | 0x054 | EHCI Port Status/Control Register |
| OHCI Control and Status Partition Register | | |
| O_HcRevision | 0x400 | OHCI Revision Register |
| O_HcControl | 0x404 | OHCI Control Register |
| O_HcCommandStatus | 0x408 | OHCI Command Status Register |
| O_HcInterruptStatus | 0x40c | OHCI Interrupt Status Register |
| O_HcInterruptEnable | 0x410 | OHCI Interrupt Enable Register |
| O_HcInterruptDisable | 0x414 | OHCI Interrupt Disable Register |
| OHCI Memory Pointer Partition Register | | |
| O_HcHCCA | 0x418 | OHCI HCCA Base |
| O_HcPeriodCurrentED | 0x41c | OHCI Period Current ED Base |
| O_HcControlHeadED | 0x420 | OHCI Control Head ED Base |
| O_HcControlCurrentED | 0x424 | OHCI Control Current ED Base |
| O_HcBulkHeadED | 0x428 | OHCI Bulk Head ED Base |
| O_HcBulkCurrentED | 0x42c | OHCI Bulk Current ED Base |
| O_HcDoneHead | 0x430 | OHCI Done Head Base |
| OHCI Frame Counter Partition Register | | |
| O_HcFmInterval | 0x434 | OHCI Frame Interval Register |
| O_HcFmRemaining | 0x438 | OHCI Frame Remaining Register |
| O_HcFmNumber | 0x43c | OHCI Frame Number Register |
| O_HcPeriodicStart | 0x440 | OHCI Periodic Start Register |
| O_HcLSThreshold | 0x444 | OHCI LS Threshold Register |
| OHCI Root Hub Partition Register | | |
| O_HcRhDescriptorA | 0x448 | OHCI Root Hub Descriptor Register A |
| O_HcRhDescriptorB | 0x44c | OHCI Root Hub Descriptor Register B |
| O_HcRhStatus | 0x450 | OHCI Root Hub Status Register |
| O_HcRhPortStatus | 0x454 | OHCI Root Hub Port Status Register |

8.4.1.3. USB OTG_EHCI Register Description

8.4.1.3.1. EHCI Identification Register(Default Value: Implementation Dependent)

| Offset: 0x0000 | | | Register Name: CAPLENGTH |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 7:0 | R | 0x10 | CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space. |

8.4.1.3.2. EHCI Host Interface Version Number Register(Default Value: 0x0100)

| Offset: 0x0002 | | | Register Name: HCVERSION |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 15:0 | R | 0x0100 | HCVERSION This is a 16-bits register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. |

8.4.1.3.3. EHCI Host Control Structural Parameter Register(Default Value: Implementation Dependent)

| Offset: 0x0004 | | | Register Name: HCSPARAMS | | | | | | |
|----------------|---|-------------|--|-------|---------|---|---|---|--|
| Bit | R/W | Default/Hex | Description | | | | | | |
| 31:24 | / | 0 | Reserved. These bits are reserved and should be set to zero. | | | | | | |
| 23:20 | R | 0 | Debug Port Number This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'. | | | | | | |
| 19:16 | / | 0 | Reserved. These bits are reserved and should be set to zero. | | | | | | |
| 15:12 | R | 0 | Number of Companion Controller (N_CC) This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'. | | | | | | |
| 11:8 | R | 0 | Number of Port per Companion Controller(N_PCC) This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software. This field will always fix with '0'. | | | | | | |
| 7 | R | 0 | Port Routing Rules This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Value</th> <th>Meaning</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on.</td> </tr> <tr> <td>1</td> <td>The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array.</td> </tr> </tbody> </table> This field will always be '0'. | Value | Meaning | 0 | The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on. | 1 | The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array. |
| Value | Meaning | | | | | | | | |
| 0 | The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on. | | | | | | | | |
| 1 | The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array. | | | | | | | | |
| 6:4 | / | 0 | Reserved. These bits are reserved and should be set to zero. | | | | | | |
| 3:0 | R | 1 | N_PORTS This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f. This field is always 1. | | | | | | |

8.4.1.3.4. EHCI Host Control Capability Parameter Register(Default Value: Implementation Dependent)

| Offset: 0x0008 | | | Register Name: HCCPARAMS |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:16 | / | 0 | Reserved These bits are reserved and should be set to zero. |
| 15:18 | R | 0 | EHCI Extended Capabilities Pointer (ECCP) |

| | | | |
|-----|---|---|--|
| | | | <p>This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain consistency of the PCI header defined for this class of device.</p> <p>The value of this field is always '00b'.</p> |
| 7:4 | R | | <p>Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures (one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.</p> |
| 3 | R | 0 | <p>Reserved These bits are reserved and should be set to zero.</p> |
| 2 | R | | <p>Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.</p> |
| 1 | R | | <p>Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1, then system software can specify and use the frame list in the USBCMD register Frame List Size field to configure the host controller. The frame list must always align on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.</p> |
| 0 | R | 0 | <p>Reserved These bits are reserved for future use and should return a value of zero when read.</p> |

8.4.1.3.5. EHCI Companion Port Route Description (Default Value: UNDEFINED)

| Offset: 0x000C | | | Register Name: HCSP-PORTROUTE |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | | <p>HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.</p> |

8.4.1.3.6. EHCI USB Command Register (Default Value: 0x00080000(0x00080B00 if Asynchronous Schedule Park Capability is a one))

| Offset: 0x0010 | | | Register Name: USBCMD | | | | | | | | | | | | | | | | | | |
|----------------|---|-------------|---|-------|----------------------------|------|----------|------|---------------|------|---------------|------|---------------|------|---|------|---------------------|------|---------------------|------|---------------------|
| Bit | R/W | Default/Hex | Description | | | | | | | | | | | | | | | | | | |
| 31:24 | / | 0 | Reserved These bits are reserved and should be set to zero. | | | | | | | | | | | | | | | | | | |
| 23:16 | R/W | 0x08 | <p>Interrupt Threshold Control The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Minimum Interrupt Interval</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Reserved</td> </tr> <tr> <td>0x01</td> <td>1 micro-frame</td> </tr> <tr> <td>0x02</td> <td>2 micro-frame</td> </tr> <tr> <td>0x04</td> <td>4 micro-frame</td> </tr> <tr> <td>0x08</td> <td>8 micro-frame(default, equates to 1 ms)</td> </tr> <tr> <td>0x10</td> <td>16 micro-frame(2ms)</td> </tr> <tr> <td>0x20</td> <td>32 micro-frame(4ms)</td> </tr> <tr> <td>0x40</td> <td>64 micro-frame(8ms)</td> </tr> </tbody> </table> <p>Any other value in this register yields undefined results. The default value in this field is 0x08 . Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.</p> | Value | Minimum Interrupt Interval | 0x00 | Reserved | 0x01 | 1 micro-frame | 0x02 | 2 micro-frame | 0x04 | 4 micro-frame | 0x08 | 8 micro-frame(default, equates to 1 ms) | 0x10 | 16 micro-frame(2ms) | 0x20 | 32 micro-frame(4ms) | 0x40 | 64 micro-frame(8ms) |
| Value | Minimum Interrupt Interval | | | | | | | | | | | | | | | | | | | | |
| 0x00 | Reserved | | | | | | | | | | | | | | | | | | | | |
| 0x01 | 1 micro-frame | | | | | | | | | | | | | | | | | | | | |
| 0x02 | 2 micro-frame | | | | | | | | | | | | | | | | | | | | |
| 0x04 | 4 micro-frame | | | | | | | | | | | | | | | | | | | | |
| 0x08 | 8 micro-frame(default, equates to 1 ms) | | | | | | | | | | | | | | | | | | | | |
| 0x10 | 16 micro-frame(2ms) | | | | | | | | | | | | | | | | | | | | |
| 0x20 | 32 micro-frame(4ms) | | | | | | | | | | | | | | | | | | | | |
| 0x40 | 64 micro-frame(8ms) | | | | | | | | | | | | | | | | | | | | |
| 15:12 | / | 0 | Reserved These bits are reserved and should be set to zero. | | | | | | | | | | | | | | | | | | |
| 11 | R/W or R | 0 | Asynchronous Schedule Park Mode Enable(OPTIONAL) If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled. | | | | | | | | | | | | | | | | | | |
| 10 | / | 0 | Reserved These bits are reserved and should be set to zero. | | | | | | | | | | | | | | | | | | |
| 9:8 | R/W or R | 0 | Asynchronous Schedule Park Mode Count(OPTIONAL) Asynchronous Park Capability bit in the HCCPARAMS register is a one, Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid value are 0x1 to 0x3. Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior. | | | | | | | | | | | | | | | | | | |
| 7 | R/W | 0 | Light Host Controller Reset(OPTIONAL) This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships). A host software read of this bit as zero indicates the Light Host Controller | | | | | | | | | | | | | | | | | | |

| | | | Reset has completed and it is safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host | | | | | | | | | | |
|-----------|--|---|--|-----------|---------|-----|---|-----|--|-----|---|-----|----------|
| 6 | R/W | 0 | <p>Interrupt on Async Advance Doorbell</p> <p>This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell.</p> <p>When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. If the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.</p> <p>Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</p> | | | | | | | | | | |
| 5 | R/W | 0 | <p>Asynchronous Schedule Enable</p> <p>This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:</p> <table border="1"> <thead> <tr> <th>Bit Value</th> <th>Meaning</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Do not process the Asynchronous Schedule.</td> </tr> <tr> <td>1</td> <td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td> </tr> </tbody> </table> <p>The default value of this field is '0b'.</p> | Bit Value | Meaning | 0 | Do not process the Asynchronous Schedule. | 1 | Use the ASYNLISTADDR register to access the Asynchronous Schedule. | | | | |
| Bit Value | Meaning | | | | | | | | | | | | |
| 0 | Do not process the Asynchronous Schedule. | | | | | | | | | | | | |
| 1 | Use the ASYNLISTADDR register to access the Asynchronous Schedule. | | | | | | | | | | | | |
| 4 | R/W | 0 | <p>Periodic Schedule Enable</p> <p>This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:</p> <table border="1"> <thead> <tr> <th>Bit Value</th> <th>Meaning</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Do not process the Periodic Schedule.</td> </tr> <tr> <td>1</td> <td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td> </tr> </tbody> </table> <p>The default value of this field is '0b'.</p> | Bit Value | Meaning | 0 | Do not process the Periodic Schedule. | 1 | Use the PERIODICLISTBASE register to access the Periodic Schedule. | | | | |
| Bit Value | Meaning | | | | | | | | | | | | |
| 0 | Do not process the Periodic Schedule. | | | | | | | | | | | | |
| 1 | Use the PERIODICLISTBASE register to access the Periodic Schedule. | | | | | | | | | | | | |
| 3:2 | R/W or R | 0 | <p>Frame List Size</p> <p>This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the Frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean:</p> <table border="1"> <thead> <tr> <th>Bits</th> <th>Meaning</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1024 elements(4096bytes)Default value</td> </tr> <tr> <td>01b</td> <td>512 elements(2048bytes)</td> </tr> <tr> <td>10b</td> <td>256 elements(1024bytes)For resource-constrained condition</td> </tr> <tr> <td>11b</td> <td>reserved</td> </tr> </tbody> </table> <p>The default value is '00b'.</p> | Bits | Meaning | 00b | 1024 elements(4096bytes)Default value | 01b | 512 elements(2048bytes) | 10b | 256 elements(1024bytes)For resource-constrained condition | 11b | reserved |
| Bits | Meaning | | | | | | | | | | | | |
| 00b | 1024 elements(4096bytes)Default value | | | | | | | | | | | | |
| 01b | 512 elements(2048bytes) | | | | | | | | | | | | |
| 10b | 256 elements(1024bytes)For resource-constrained condition | | | | | | | | | | | | |
| 11b | reserved | | | | | | | | | | | | |
| 1 | R/W | 0 | <p>Host Controller Reset</p> <p>This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports.</p> <p>All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to</p> | | | | | | | | | | |

| | | | |
|---|-----|---|--|
| | | | <p>an operational state.</p> <p>This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.</p> <p>Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.</p> |
| 0 | R/W | 0 | <p>Run/Stop</p> <p>When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State.</p> <p>The default value is 0x0.</p> |

8.4.1.3.7. EHCI USB Status Register (Default Value: 0x00001000)

| Offset: 0x0014 | | | Register Name: USBSTS |
|----------------|------|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | / | 0 | <p>Reserved</p> <p>These bits are reserved and should be set to zero.</p> |
| 15 | R | 0 | <p>Asynchronous Schedule Status</p> <p>The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).</p> |
| 14 | R | 0 | <p>Periodic Schedule Status</p> <p>The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).</p> |
| 13 | R | 0 | <p>Reclamation</p> <p>This is a read-only status bit, which is used to detect an empty asynchronous schedule.</p> |
| 12 | R | 1 | <p>HC Halted</p> <p>This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error).</p> <p>The default value is '1'.</p> |
| 11:6 | / | 0 | <p>Reserved</p> <p>These bits are reserved and should be set to zero.</p> |
| 5 | R/WC | 0 | <p>Interrupt on Async Advance</p> |

| | | | |
|---|------|---|--|
| | | | System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source. |
| 4 | R/WC | 0 | <p>Host System Error</p> <p>The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.</p> |
| 3 | R/WC | 0 | <p>Frame List Rollover</p> <p>The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.</p> |
| 2 | R/WC | 0 | <p>Port Change Detect</p> <p>The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.</p> |
| 1 | R/WC | 0 | <p>USB Error Interrupt(USBERRINT)</p> <p>The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.</p> |
| 0 | R/WC | 0 | <p>USB Interrupt(USBINT)</p> <p>The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set.</p> <p>The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)</p> |

8.4.1.3.8. EHCI USB Interrupt Enable Register (Default Value: 0x00000000)

| Offset: 0x0018 | | | Register Name: USBINTR |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:6 | / | 0 | Reserved These bits are reserved and should be zero. |
| 5 | R/W | 0 | <p>Interrupt on Async Advance Enable</p> <p>When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.</p> |
| 4 | R/W | 0 | <p>Host System Error Enable</p> <p>When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.</p> |
| 3 | R/W | 0 | Frame List Rollover Enable |

| | | | |
|---|-----|---|---|
| | | | When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit. |
| 2 | R/W | 0 | Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit. |
| 1 | R/W | 0 | USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit. |
| 0 | R/W | 0 | USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit. |

8.4.1.3.9. EHCI Frame Index Register (Default Value: 0x00000000)

| Offset: 0x001C | | | Register Name: FRINDEX | | |
|----------------|-----|-------------|---|-----------------|----|
| Bit | R/W | Default/Hex | Description | | |
| 31:14 | / | 0 | Reserved These bits are reserved and should be zero. | | |
| 13:0 | R/W | 0 | Frame Index The value in this register increment at the end of each time frame (e.g. micro-frame). Bits[N:3] are used for the Frame List current index. It Means that each location of the frame list is accessed 8 times(frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register. | | |
| | | | USBCMD[Frame List Size] | Number Elements | N |
| | | | 00b | 1024 | 12 |
| | | | 01b | 512 | 11 |
| | | | 10b | 256 | 10 |
| | | | 11b | Reserved | |

Note: This register must be written as a DWord. Byte writes produce undefined results.

8.4.1.3.10. EHCI Periodic Frame List Base Address Register (Default Value: Undefined)

| Offset: 0x0024 | | | Register Name: PERIODICLISTBASE |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:12 | R/W | | Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence. |
| 11:0 | / | | Reserved Must be written as 0x0 during runtime, the values of these bits are |

| | | | |
|--|--|--|------------|
| | | | undefined. |
|--|--|--|------------|

Note: Writes must be Dword Writes.

8.4.1.3.11. EHCI Current Asynchronous List Address Register (Default Value: Undefined)

| Offset: 0x0028 | | | Register Name: ASYNCLISTADDR |
|----------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:5 | R/W | | Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively. |
| 4:0 | / | / | Reserved These bits are reserved and their value has no effect on operation. Bits in this field cannot be modified by system software and will always return a zero when read. |

Note: Write must be DWord Writes.

8.4.1.3.12. EHCI Configure Flag Register (Default Value: 0x00000000)

| Offset: 0x0050 | | | Register Name: CONFIGFLAG | | | | | | |
|----------------|--|-------------|---|-------|---------|---|--|---|---|
| Bit | R/W | Default/Hex | Description | | | | | | |
| 31:1 | / | 0 | Reserved These bits are reserved and should be set to zero. | | | | | | |
| 0 | R/W | 0 | Configure Flag(CF) Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Value</th> <th>Meaning</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Port routing control logic default-routs each port to an implementation dependent classic host controller.</td> </tr> <tr> <td>1</td> <td>Port routing control logic default-routs all ports to this host controller.</td> </tr> </tbody> </table> The default value of this field is '0'. | Value | Meaning | 0 | Port routing control logic default-routs each port to an implementation dependent classic host controller. | 1 | Port routing control logic default-routs all ports to this host controller. |
| Value | Meaning | | | | | | | | |
| 0 | Port routing control logic default-routs each port to an implementation dependent classic host controller. | | | | | | | | |
| 1 | Port routing control logic default-routs all ports to this host controller. | | | | | | | | |

Note: This register is not use in the normal implementation.

8.4.1.3.13. EHCI Port Status and Control Register (Default Value: 0x00002000(w/PPC set to one);0x00003000

(w/PPC set to a zero))

| Offset: 0x0054 | | | Register Name: PORTSC |
|----------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:22 | / | 0 | Reserved These bits are reserved for future use and should return a value of zero when read. |
| 21 | R/W | 0 | Wake on Disconnect Enable(WKDSCNNT_E) Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. |

| | | | This field is zero if Port Power is zero. The default value in this field is '0'. | | | | | | | | | | | | | | | | |
|---------------|---|--|---|------------|-----------|----------------|---|-------|---|-------|--------------|---|--------------|---------|--|-------|-------------------|---|----------|
| 20 | R/W | 0 | Wake on Connect Enable(WKCNNT_E) Writing this bit to a one enable the port to be sensitive to device connects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'. | | | | | | | | | | | | | | | | |
| 19:16 | R/W | 0 | Port Test Control The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follow: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Test Mode</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>The port is NOT operating in a test mode.</td> </tr> <tr> <td>0001b</td> <td>Test J_STATE</td> </tr> <tr> <td>0010b</td> <td>Test K_STATE</td> </tr> <tr> <td>0011b</td> <td>Test SEO_NAK</td> </tr> <tr> <td>0100b</td> <td>Test Packet</td> </tr> <tr> <td>0101b</td> <td>Test FORCE_ENABLE</td> </tr> <tr> <td>0110b - 1111b</td> <td>Reserved</td> </tr> </tbody> </table> <p>The default value in this field is '0000b'.</p> | Bits | Test Mode | 0000b | The port is NOT operating in a test mode. | 0001b | Test J_STATE | 0010b | Test K_STATE | 0011b | Test SEO_NAK | 0100b | Test Packet | 0101b | Test FORCE_ENABLE | 0110b - 1111b | Reserved |
| Bits | Test Mode | | | | | | | | | | | | | | | | | | |
| 0000b | The port is NOT operating in a test mode. | | | | | | | | | | | | | | | | | | |
| 0001b | Test J_STATE | | | | | | | | | | | | | | | | | | |
| 0010b | Test K_STATE | | | | | | | | | | | | | | | | | | |
| 0011b | Test SEO_NAK | | | | | | | | | | | | | | | | | | |
| 0100b | Test Packet | | | | | | | | | | | | | | | | | | |
| 0101b | Test FORCE_ENABLE | | | | | | | | | | | | | | | | | | |
| 0110b - 1111b | Reserved | | | | | | | | | | | | | | | | | | |
| 15:14 | R/W | 0 | Reserved These bits are reserved for future use and should return a value of zero when read. | | | | | | | | | | | | | | | | |
| 13 | R/W | 1 | Port Owner This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero. System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. Default Value = 1b. | | | | | | | | | | | | | | | | |
| 12 | / | 0 | Reserved These bits are reserved for future use and should return a value of zero when read. | | | | | | | | | | | | | | | | |
| 11:10 | R | 0 | Line Status These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bit[11:10]</th> <th>USB State</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>SEO</td> <td>Not Low-speed device, perform EHCI reset.</td> </tr> <tr> <td>10b</td> <td>J-state</td> <td>Not Low-speed device, perform EHCI reset.</td> </tr> <tr> <td>01b</td> <td>K-state</td> <td>Low-speed device, release ownership of port.</td> </tr> <tr> <td>11b</td> <td>Undefined</td> <td>Not Low-speed device, perform EHCI reset.</td> </tr> </tbody> </table> | Bit[11:10] | USB State | Interpretation | 00b | SEO | Not Low-speed device, perform EHCI reset. | 10b | J-state | Not Low-speed device, perform EHCI reset. | 01b | K-state | Low-speed device, release ownership of port. | 11b | Undefined | Not Low-speed device, perform EHCI reset. | |
| Bit[11:10] | USB State | Interpretation | | | | | | | | | | | | | | | | | |
| 00b | SEO | Not Low-speed device, perform EHCI reset. | | | | | | | | | | | | | | | | | |
| 10b | J-state | Not Low-speed device, perform EHCI reset. | | | | | | | | | | | | | | | | | |
| 01b | K-state | Low-speed device, release ownership of port. | | | | | | | | | | | | | | | | | |
| 11b | Undefined | Not Low-speed device, perform EHCI reset. | | | | | | | | | | | | | | | | | |

| | | | This value of this field is undefined if Port Power is zero. | | | | | | | | |
|-----------------------------|------------|---|--|-----------------------------|------------|----|---------|----|--------|----|---------|
| 9 | / | 0 | Reserved This bit is reserved for future use, and should return a value of zero when read. | | | | | | | | |
| 8 | R/W | 0 | Port Reset 1=Port is in Reset. 0=Port is not in Reset. Default value = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Notes: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero. The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one. This field is zero if Port Power is zero. | | | | | | | | |
| 7 | R/W | 0 | Suspend Port Enabled Bit and Suspend bit of this register define the port states as follows: <table border="1"> <thead> <tr> <th>Bits[Port Enables, Suspend]</th> <th>Port State</th> </tr> </thead> <tbody> <tr> <td>0x</td> <td>Disable</td> </tr> <tr> <td>10</td> <td>Enable</td> </tr> <tr> <td>11</td> <td>Suspend</td> </tr> </tbody> </table> When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when: <ol style="list-style-type: none"> ① Software sets the Force Port Resume bit to a zero(from a one). ② Software sets the Port Reset bit to a one(from a zero). If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined. This field is zero if Port Power is zero. The default value in this field is '0'. | Bits[Port Enables, Suspend] | Port State | 0x | Disable | 10 | Enable | 11 | Suspend |
| Bits[Port Enables, Suspend] | Port State | | | | | | | | | | |
| 0x | Disable | | | | | | | | | | |
| 10 | Enable | | | | | | | | | | |
| 11 | Suspend | | | | | | | | | | |
| 6 | R/W | 0 | Force Port Resume 1 = Resume detected/driven on port. 0 = No resume (K-state) detected/ driven on port. Default value = 0. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined. | | | | | | | | |

| | | | |
|---|------|---|--|
| | | | <p>Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit.</p> <p>Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.</p> |
| 5 | R/WC | 0 | <p>Over-current Change Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.</p> |
| 4 | R | 0 | <p>Over-current Active 0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.</p> |
| 3 | R/WC | 0 | <p>Port Enable/Disable Change Default = 0. 1 = Port enabled/disabled status has changed. 0 = No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.</p> |
| 2 | R/W | 0 | <p>Port Enabled/Disabled 1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.</p> |
| 1 | R/WC | 0 | <p>Connect Status Change 1=Change in Current Connect Status, 0=No change, Default=0. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.</p> |
| 0 | R | 0 | <p>Current Connect Status Device is present on port when the value of this field is a one, and no device</p> |

| | | | |
|--|--|--|--|
| | | | is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero. |
|--|--|--|--|

Note: This register is only reset by hardware or in response to a host controller reset.

8.4.1.4. USB OTG_OHCI Register Description

8.4.1.4.1. HcRevision Register(Default Value: 0x00000010)

| Offset: 0x400 | | | | Register Name: HcRevision |
|---------------|------------|----|-------------|---|
| | Read/Write | | | |
| Bit | HCD | HC | Default/HEX | Description |
| 31:8 | / | / | 0x00 | Reserved |
| 7:0 | R | R | 0x10 | Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10. |

8.4.1.4.2. HcControl Register(Default Value: 0x00000000)

| Offset: 0x404 | | | | Register Name: HcRevision |
|---------------|------------|-----|-------------|---|
| | Read/Write | | | |
| Bit | HCD | HC | Default/HEX | Description |
| 31:11 | / | / | 0x00 | Reserved |
| 10 | R/W | R | 0x0 | RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt. |
| 9 | R/W | R/W | 0x0 | RemoteWakeupConnected This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification. |
| 8 | R/W | R | 0x0 | InterruptRouting This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC. |
| 7:6 | R/W | R/W | 0x0 | HostControllerFunctionalState for USB |

| | | | | <table border="1"> <tr> <td>00b</td> <td>USBReset</td> </tr> <tr> <td>01b</td> <td>USBResume</td> </tr> <tr> <td>10b</td> <td>USBOperational</td> </tr> <tr> <td>11b</td> <td>USBSuspend</td> </tr> </table> <p>A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus.</p> <p>This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port.</p> <p>HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.</p> | 00b | USBReset | 01b | USBResume | 10b | USBOperational | 11b | USBSuspend |
|------|---|---|-----|--|------|---|-----|-----------|-----|----------------|-----|------------|
| 00b | USBReset | | | | | | | | | | | |
| 01b | USBResume | | | | | | | | | | | |
| 10b | USBOperational | | | | | | | | | | | |
| 11b | USBSuspend | | | | | | | | | | | |
| 5 | R/W | R | 0x0 | <p>BulkListEnable</p> <p>This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.</p> | | | | | | | | |
| 4 | R/W | R | 0x0 | <p>ControlListEnable</p> <p>This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.</p> | | | | | | | | |
| 3 | R/W | R | 0x0 | <p>IsochronousEnable</p> <p>This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists.</p> <p>Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).</p> | | | | | | | | |
| 2 | R/W | R | 0x0 | <p>PeriodicListEnable</p> <p>This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.</p> | | | | | | | | |
| 1:0 | R/W | R | 0x0 | <p>ControlBulkServiceRatio</p> <p>This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.</p> <table border="1"> <thead> <tr> <th>CBSR</th> <th>No. of Control EDs Over Bulk EDs Served</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1:1</td> </tr> <tr> <td>1</td> <td>2:1</td> </tr> <tr> <td>2</td> <td>3:1</td> </tr> </tbody> </table> | CBSR | No. of Control EDs Over Bulk EDs Served | 0 | 1:1 | 1 | 2:1 | 2 | 3:1 |
| CBSR | No. of Control EDs Over Bulk EDs Served | | | | | | | | | | | |
| 0 | 1:1 | | | | | | | | | | | |
| 1 | 2:1 | | | | | | | | | | | |
| 2 | 3:1 | | | | | | | | | | | |

| | | | | | |
|---------------------------|--|--|--|---|-----|
| | | | | 3 | 4:1 |
| The default value is 0x0. | | | | | |

8.4.1.4.3. HcCommandStatus Register(Default Value: 0x00000000)

| Offset: 0x408 | | | | Register Name: HcCommandStatus |
|---------------|------------|-----|-------------|---|
| Bit | Read/Write | | Default/HEX | Description |
| | HCD | HC | | |
| 31:18 | / | / | 0x0 | Reserved |
| 17:16 | R | R/W | 0x0 | SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problem. |
| 15:4 | / | / | 0x0 | Reserved |
| 3 | R/W | R/W | 0x0 | OwenshipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwenshipChange field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from OS HCD. |
| 2 | R/W | R/W | 0x0 | BulkListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop. |
| 1 | R/W | R/W | 0x0 | ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop. |
| 0 | R/W | R/E | 0x0 | HostControllerReset This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBsuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InterruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports. |

8.4.1.4.4. HcInterruptStatus Register(Default Value: 0x00000000)

| Offset: 0x40c | | | | Register Name: HcInterruptStatus |
|---------------|------------|-----|-------------|--|
| Bit | Read/Write | | Default/HEX | Description |
| | HCD | HC | | |
| 31:7 | / | / | 0x0 | Reserved |
| 6 | R/W | R/W | 0x0 0x1 ? | RootHubStatusChange This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed. |
| 5 | R/W | R/W | 0x0 | FrameNumberOverflow This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated. |
| 4 | R/W | R/W | 0x0 | UnrecoverableError This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset. |
| 3 | R/W | R/W | 0x0 | ResumeDetected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state. |
| 2 | R/W | R/W | 0x0 | StartofFrame This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time. |
| 1 | R/W | R/W | 0x0 | WritebackDoneHead This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead. |
| 0 | R/W | R/W | 0x0 | SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be Incremented. |

8.4.1.4.5. HcInterruptEnable Register(Default Value: 0x00000000)

| Offset: 0x410 | | | | Register Name: HcInterruptEnable Register | |
|---------------|------------|----|---------|--|--|
| Bit | Read/Write | | Default | Description | |
| | HCD | HC | | | |
| 31 | R/W | R | 0x0 | MasterInterruptEnable A '0' writtern to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable. | |
| 30:7 | / | / | 0x0 | Reserved | |
| 6 | R/W | R | 0x0 | RootHubStatusChange Interrupt Enable | |
| | | | | 0 | Ignore; |
| | | | | 1 | Enable interrupt generation due to Root Hub Status Change; |

| | | | | |
|---|-----|---|-----|--------------------------------------|
| | | | | |
| 5 | R/W | R | 0x0 | FrameNumberOverflow Interrupt Enable |
| | | | | 0 |
| | | | | |
| 4 | R/W | R | 0x0 | UnrecoverableError Interrupt Enable |
| | | | | 0 |
| | | | | |
| 3 | R/W | R | 0x0 | ResumeDetected Interrupt Enable |
| | | | | 0 |
| | | | | |
| 2 | R/W | R | 0x0 | StartofFrame Interrupt Enable |
| | | | | 0 |
| | | | | |
| 1 | R/W | R | 0x0 | WritebackDoneHead Interrupt Enable |
| | | | | 0 |
| | | | | |
| 0 | R/W | R | 0x0 | SchedulingOverrun Interrupt Enable |
| | | | | 0 |

8.4.1.4.6. HcInterruptDisable Register(Default Value: 0x00000000)

| Offset: 0x414 | | | | Register Name: HcInterruptDisable Register |
|---------------|------------|----|-------------|---|
| Bit | Read/Write | | Default/HEX | Description |
| | HCD | HC | | |
| 31 | R/W | R | 0x0 | MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset. |
| 30:7 | / | / | 0x00 | Reserved |
| 6 | R/W | R | 0x0 | RootHubStatusChange Interrupt Disable |
| | | | | 0 |
| | | | | |
| 5 | R/W | R | 0x0 | FrameNumberOverflow Interrupt Disable |
| | | | | 0 |
| | | | | |
| 4 | R/W | R | 0x0 | UnrecoverableError Interrupt Disable |
| | | | | 0 |
| | | | | |
| 3 | R/W | R | 0x0 | ResumeDetected Interrupt Disable |
| | | | | 0 |
| | | | | |
| 2 | R/W | R | 0x0 | StartofFrame Interrupt Disable |
| | | | | 0 |

| | | | | | |
|---|-----|---|-----|-------------------------------------|---|
| | | | | | |
| 1 | R/W | R | 0x0 | WritebackDoneHead Interrupt Disable | |
| | | | | 0 | Ignore; |
| | | | | | |
| 0 | R/w | R | 0x0 | SchedulingOverrun Interrupt Disable | |
| | | | | 0 | Ignore; |
| | | | | | |
| | | | | 1 | Disable interrupt generation due to Scheduling Overrun; |

8.4.1.4.7. HcHCCA Register(Default Value: 0x00000000)

| Offset: 0x418 | | | | Register Name: HcHCCA |
|---------------|------------|----|-------------|--|
| Bit | Read/Write | | Default/HEX | Description |
| | HCD | HC | | |
| 31:8 | R/W | R | 0x0 | HCCA[31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver. |
| 7:0 | R | R | 0x0 | HCCA[7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read. |

8.4.1.4.8. HcPeriodCurrentED Register(Default Value: 0x00000000)

| Offset: 0x41c | | | | Register Name: HcPeriodCurrentED(PCED) |
|---------------|------------|-----|-------------|--|
| Bit | Read/Write | | Default/HEX | Description |
| | HCD | HC | | |
| 31:4 | R | R/W | 0x0 | PCED[31:4] This is used by HC to point to the head of one of the Periodic ED list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading. |
| 3:0 | R | R | 0x0 | PCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field. |

8.4.1.4.9. HcControlHeadED Register(Default Value: 0x00000000)

| Offset: 0x420 | | | | Register Name: HcControlHeadED[CHED] |
|---------------|------------|----|-------------|---|
| Bit | Read/Write | | Default/HEX | Description |
| | HCD | HC | | |
| 31:4 | R/W | R | 0x0 | EHCD[31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list |

| | | | | |
|-----|---|---|-----|--|
| | | | | starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC. |
| 3:0 | R | R | 0x0 | EHCD[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field. |

8.4.1.4.10. HcControlCurrentED Register(Default Value: 0x00000000)

| | | | | |
|---------------|------------|-----|-------------|--|
| Offset: 0x424 | | | | Register Name: HcControlCurrentED[CCED] |
| Bit | Read/Write | | Default/Hex | Description |
| | HCD | HC | | |
| 31:4 | R/W | R/W | 0x0 | CCED[31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list. |
| 3:0 | R | R | 0x0 | CCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field. |

8.4.1.4.11. HcBulkHeadED Register(Default Value: 0x00000000)

| | | | | |
|---------------|------------|----|-------------|--|
| Offset: 0x428 | | | | Register Name: HcBulkHeadED[BHED] |
| Bit | Read/Write | | Default/HEX | Description |
| | HCD | HC | | |
| 31:4 | R/W | R | 0x0 | BHED[31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC. |
| 3:0 | R | R | 0x0 | BHED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field. |

8.4.1.4.12. HcBulkCurrentED Register(Default Value: 0x00000000)

| | | | |
|---------------|------------|-------------|--|
| Offset: 0x42c | | | Register Name: HcBulkCurrentED [BCED] |
| Bit | Read/Write | Default/HEX | Description |

| | HCD | HC | | |
|------|-----|-----|-----|---|
| 31:4 | R/W | R/W | 0x0 | BulkCurrentED[31:4] This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControllistFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list. |
| 3:0 | R | R | 0x0 | BulkCurrentED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field. |

8.4.1.4.13. HcDoneHead Register(Default Value: 0x00000000)

| Offset: 0x430 | | | | Register Name: HcDoneHead |
|---------------|------------|-----|-------------|---|
| Bit | Read/Write | | Default/Hex | Description |
| | HCD | HC | | |
| 31:4 | R | R/W | 0x0 | HcDoneHead[31:4] When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus. |
| 3:0 | R | R | 0x0 | HcDoneHead[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field. |

8.4.1.4.14. HcFmInterval Register(Default Value: 0x00002EDF)

| Offset: 0x434 | | | | Register Name: HcFmInterval Register |
|---------------|------------|----|-------------|---|
| Bit | Read/Write | | Default/Hex | Description |
| | HCD | HC | | |
| 31 | R/W | R | 0x0 | FrameIntervalToggler HCD toggles this bit whenever it loads a new value to FrameInterval. |
| 30:16 | R/W | R | 0x0 | FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD. |
| 15:14 | / | / | 0x0 | Reserved |
| 13:0 | R/W | R | 0x2edf | FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of |

| | | | | |
|--|--|--|--|---|
| | | | | HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence. |
|--|--|--|--|---|

8.4.1.4.15. HcFmRemaining Register(Default Value: 0x00000000)

| Offset: 0x438 | | | | Register Name: HcFmRemaining |
|---------------|------------|-----|-------------|---|
| Bit | Read/Write | | Default/Hex | Description |
| | HCD | HC | | |
| 31 | R | R/W | 0x0 | FrameRemaining Toggle This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining. |
| 30:14 | / | / | 0x0 | Reserved |
| 13:0 | R | RW | 0x0 | FramRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of HcFmInterval and uses the updated value from the next SOF. |

8.4.1.4.16. HcFmNumber Register(Default Value: 0x00000000)

| Offset: 0x43c | | | | Register Name: HcFmNumber |
|---------------|------------|-----|-------------|--|
| Bit | Read/Write | | Default/Hex | Description |
| | HCD | HC | | |
| 31:16 | | | | Reserved |
| 15:0 | R | R/W | 0x0 | FrameNumber This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0x0 after 0x0fff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus. |

8.4.1.4.17. HcPeriodicStart Register(Default Value: 0x00000000)

| Offset: 0x440 | | | | Register Name: HcPeriodicStatus |
|---------------|------------|----|-------------|---|
| Bit | Read/Write | | Default/Hex | Description |
| | HCD | HC | | |
| 31:14 | | | | Reserved |
| 13:0 | R/W | R | 0x0 | PeriodicStart After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 0x2A3F (0x3e67??). When HcFmRemaining reaches the value specified, processing of the periodic |

| | | | | |
|--|--|--|--|--|
| | | | | lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress. |
|--|--|--|--|--|

8.4.1.4.18. HcLSThreshold Register(Default Value: 0x0000628)

| Offset: 0x444 | | | Register Name: HcLSThreshold | |
|---------------|------------|----|-------------------------------------|--|
| Bit | Read/Write | | Default/Hex | Description |
| | HCD | HC | | |
| 31:12 | | | | Reserved |
| 11:0 | R/W | R | 0x0628 | LSThreshold This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ³ this field. The value is calculated by HCD with the consideration of transmission and setup overhead. |

8.4.1.4.19. HcRhDescriptorA Register(Default Value: 0x02001201)

| Offset: 0x448 | | | Register Name: HcRhDescriptorA | |
|---------------|--|----|---------------------------------------|--|
| Bit | Read/Write | | Default/Hex | Description |
| | HCD | HC | | |
| 31:24 | R/W | R | 0x2 | PowerOnToPowerGoodTime[POTPGT] This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms. |
| 23:13 | | | | Reserved |
| 12 | R/W | R | 1 | NoOverCurrentProtection This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. |
| | | | | <table border="1"> <tr> <td>0</td> <td>Over-current status is reported collectively for all downstream ports.</td> </tr> <tr> <td>1</td> <td>No overcurrent protection supported.</td> </tr> </table> |
| 0 | Over-current status is reported collectively for all downstream ports. | | | |
| 1 | No overcurrent protection supported. | | | |
| 11 | R/W | R | 0 | OverCurrentProtectionMode This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. |
| | | | | <table border="1"> <tr> <td>0</td> <td>Over-current status is reported collectively for all downstream ports.</td> </tr> <tr> <td>1</td> <td>Over-current status is reported on per-port basis.</td> </tr> </table> |
| 0 | Over-current status is reported collectively for all downstream ports. | | | |
| 1 | Over-current status is reported on per-port basis. | | | |
| 10 | R | R | 0x0 | Device Type This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0. |
| 9 | R/W | R | 1 | PowerSwitchingMode This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the |

| | | | | | | | | |
|-----|---|---|------|---|---|---|---|---|
| | | | | <p>NoPowerSwitching field is cleared.</p> <table border="1"> <tr> <td>0</td> <td>All ports are powered at the same time.</td> </tr> <tr> <td>1</td> <td>Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).</td> </tr> </table> | 0 | All ports are powered at the same time. | 1 | Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower). |
| 0 | All ports are powered at the same time. | | | | | | | |
| 1 | Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower). | | | | | | | |
| 8 | R/W | R | 0 | <p>NoPowerSwitching</p> <p>These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching.</p> <table border="1"> <tr> <td>0</td> <td>Ports are power switched.</td> </tr> <tr> <td>1</td> <td>Ports are always powered on when the HC is powered on.</td> </tr> </table> | 0 | Ports are power switched. | 1 | Ports are always powered on when the HC is powered on. |
| 0 | Ports are power switched. | | | | | | | |
| 1 | Ports are always powered on when the HC is powered on. | | | | | | | |
| 7:0 | R | R | 0x01 | <p>NumberDownstreamPorts</p> <p>These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.</p> | | | | |

8.4.1.4.20. HcRhDescriptorB Register(Default Value: 0x00000000)

| Offset: 0x44c | | | | Register Name: HcRhDescriptorB Register | |
|---------------|--------------------------------|----|-------------|---|-------------------------------|
| Bit | Read/Write | | Default/Hex | Description | |
| | HCD | HC | | | |
| 31:16 | R/W | R | 0x0 | PortPowerControlMask | |
| | | | | Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid. | |
| | | | | Bit0 | Reserved |
| | | | | Bit1 | Ganged-power mask on Port #1. |
| | | | | Bit2 | Ganged-power mask on Port #2. |
| ... | | | | | |
| Bit15 | Ganged-power mask on Port #15. | | | | |
| 15:0 | R/W | R | 0x0 | DeviceRemovable | |
| | | | | Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. | |
| | | | | Bit0 | Reserved |
| | | | | Bit1 | Device attached to Port #1. |
| | | | | Bit2 | Device attached to Port #2. |
| ... | | | | | |
| Bit15 | Device attached to Port #15. | | | | |

8.4.1.4.21. HcRhStatus Register(Default Value: 0x00000000)

| Offset: 0x450 | | | | Register Name: HcRhStatus Register | | | | |
|---------------|---|-----|-------------|---|---|---|---|---|
| Bit | Read/Write | | Default/Hex | Description | | | | |
| | HCD | HC | | | | | | |
| 31 | W | R | 0 | (write)ClearRemoteWakeupEnable Write a '1' clears DeviceRemoteWakeupEnable. Write a '0' has no effect. | | | | |
| 30:18 | / | / | 0x0 | Reserved | | | | |
| 17 | R/W | R | 0 | OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the OverCurrentIndicator field of this register. The HCD clears this bit by writing a '1'.Writing a '0' has no effect. | | | | |
| 16 | R/W | R | 0x0 | (read)LocalPowerStartusChange The Root Hub does not support the local power status features, thus, this bit is always read as '0'. (write)SetGlobalPower In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect. | | | | |
| 15 | R/W | R | 0x0 | (read)DeviceRemoteWakeupEnable This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. <table border="1" style="margin-left: 20px;"> <tr> <td>0</td> <td>ConnectStatusChange is not a remote wakeup event.</td> </tr> <tr> <td>1</td> <td>ConnectStatusChange is a remote wakeup event.</td> </tr> </table> (write)SetRemoteWakeupEnable Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect. | 0 | ConnectStatusChange is not a remote wakeup event. | 1 | ConnectStatusChange is a remote wakeup event. |
| 0 | ConnectStatusChange is not a remote wakeup event. | | | | | | | |
| 1 | ConnectStatusChange is a remote wakeup event. | | | | | | | |
| 14:2 | | | | Reserved | | | | |
| 1 | R | R/W | 0x0 | OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0' | | | | |
| 0 | R/W | R | 0x0 | (Read)LocalPowerStatus When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (Write)ClearGlobalPower When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect. | | | | |

8.4.1.4.22. HcRhPortStatus Register(Default Value: 0x00000100)

| Offset: 0x454 | Register Name: HcRhPortStatus |
|---------------|--------------------------------------|
|---------------|--------------------------------------|

| Bit | Read/Write | | Default/Hex | Description | | | | |
|-------|--------------------------------------|-----|-------------|--|---------------------------------------|---------------------------------------|---|--------------------------------------|
| | HCD | HC | | | | | | |
| 31:21 | / | / | 0x0 | Reserved | | | | |
| 20 | R/W | R/W | 0x0 | <p>PortResetStatusChange</p> <p>This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.</p> <table border="1"> <tr> <td>0</td> <td>port reset is not complete</td> </tr> <tr> <td>1</td> <td>port reset is complete</td> </tr> </table> | 0 | port reset is not complete | 1 | port reset is complete |
| | | | | 0 | port reset is not complete | | | |
| 1 | port reset is complete | | | | | | | |
| 19 | R/W | R/W | 0x0 | <p>PortOverCurrentIndicatorChange</p> <p>This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.</p> <table border="1"> <tr> <td>0</td> <td>no change in PortOverCurrentIndicator</td> </tr> <tr> <td>1</td> <td>PortOverCurrentIndicator has changed</td> </tr> </table> | 0 | no change in PortOverCurrentIndicator | 1 | PortOverCurrentIndicator has changed |
| | | | | 0 | no change in PortOverCurrentIndicator | | | |
| 1 | PortOverCurrentIndicator has changed | | | | | | | |
| 18 | R/W | R/W | 0x0 | <p>PortSuspendStatusChange</p> <p>This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resynchronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set.</p> <table border="1"> <tr> <td>0</td> <td>resume is not completed</td> </tr> <tr> <td>1</td> <td>resume completed</td> </tr> </table> | 0 | resume is not completed | 1 | resume completed |
| | | | | 0 | resume is not completed | | | |
| 1 | resume completed | | | | | | | |
| 17 | R/W | R/W | 0x0 | <p>PortEnableStatusChange</p> <p>This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.</p> <table border="1"> <tr> <td>0</td> <td>no change in PortEnableStatus</td> </tr> <tr> <td>1</td> <td>change in PortEnableStatus</td> </tr> </table> | 0 | no change in PortEnableStatus | 1 | change in PortEnableStatus |
| | | | | 0 | no change in PortEnableStatus | | | |
| 1 | change in PortEnableStatus | | | | | | | |
| 16 | R/W | R/W | 0x0 | <p>ConnectStatusChange</p> <p>This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.</p> <table border="1"> <tr> <td>0</td> <td>no change in PortEnableStatus</td> </tr> <tr> <td>1</td> <td>change in PortEnableStatus</td> </tr> </table> <p>Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.</p> | 0 | no change in PortEnableStatus | 1 | change in PortEnableStatus |
| | | | | 0 | no change in PortEnableStatus | | | |
| 1 | change in PortEnableStatus | | | | | | | |
| 15:10 | / | / | 0x0 | Reserved | | | | |
| 9 | R/W | R/W | - | <p>(read)LowSpeedDeviceAttached</p> <p>This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.</p> <table border="1"> <tr> <td>0</td> <td>full speed device attached</td> </tr> <tr> <td>1</td> <td>low speed device attached</td> </tr> </table> | 0 | full speed device attached | 1 | low speed device attached |
| | | | | 0 | full speed device attached | | | |
| 1 | low speed device attached | | | | | | | |
| | | | | (write)ClearPortPower | | | | |

| | | | | | | | | |
|-----|---------------------------------|-----|-----|---|---|---------------------------------|---|---------------------------------|
| | | | | <p>The HCD clears the PortPowerStatus bit by writing a '1' to this bit. Writing a '0' has no effect.</p> | | | | |
| | | | | <p>(read)PortPowerStatus This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.</p> <table border="1"> <tr> <td>0</td> <td>port power is off</td> </tr> <tr> <td>1</td> <td>port power is on</td> </tr> </table> <p>(write)SetPortPower The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect.</p> | 0 | port power is off | 1 | port power is on |
| 0 | port power is off | | | | | | | |
| 1 | port power is on | | | | | | | |
| 8 | R/W | R/W | 0x1 | Note: This bit is always reads '1b' if power switching is not supported. | | | | |
| 7:5 | / | / | 0x0 | Reserved | | | | |
| | | | | <p>(read)PortResetStatus When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.</p> <table border="1"> <tr> <td>0</td> <td>port reset signal is not active</td> </tr> <tr> <td>1</td> <td>port reset signal is active</td> </tr> </table> <p>(write)SetPortReset The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</p> | 0 | port reset signal is not active | 1 | port reset signal is active |
| 0 | port reset signal is not active | | | | | | | |
| 1 | port reset signal is active | | | | | | | |
| 4 | R/W | R/W | 0x0 | | | | | |
| | | | | <p>(read)PortOverCurrentIndicator This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.</p> <table border="1"> <tr> <td>0</td> <td>no overcurrent condition.</td> </tr> <tr> <td>1</td> <td>overcurrent condition detected.</td> </tr> </table> <p>(write)ClearSuspendStatus The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if PortSuspendStatus is set.</p> | 0 | no overcurrent condition. | 1 | overcurrent condition detected. |
| 0 | no overcurrent condition. | | | | | | | |
| 1 | overcurrent condition detected. | | | | | | | |
| 3 | R/W | R/W | 0x0 | | | | | |
| | | | | <p>(read)PortSuspendStatus This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when</p> | | | | |
| 2 | R/W | R/W | 0x0 | | | | | |

| | | | | | | | | |
|---|-----------------------|-----|-----|--|---|-----------------------|---|-------------------|
| | | | | <p>PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.</p> <table border="1"> <tr> <td>0</td> <td>port is not suspended</td> </tr> <tr> <td>1</td> <td>port is suspended</td> </tr> </table> <p>(write)SetPortSuspend The HCD sets the PortSuspendStatus bit by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</p> | 0 | port is not suspended | 1 | port is suspended |
| 0 | port is not suspended | | | | | | | |
| 1 | port is suspended | | | | | | | |
| 1 | R/W | R/W | 0x0 | <p>(read)PortEnableStatus This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set.</p> <table border="1"> <tr> <td>0</td> <td>port is disabled</td> </tr> <tr> <td>1</td> <td>port is enabled</td> </tr> </table> <p>(write)SetPortEnable The HCD sets PortEnableStatus by writing a '1'. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.</p> | 0 | port is disabled | 1 | port is enabled |
| 0 | port is disabled | | | | | | | |
| 1 | port is enabled | | | | | | | |
| 0 | R/W | R/W | 0x0 | <p>(read)CurrentConnectStatus This bit reflects the current state of the downstream port.</p> <table border="1"> <tr> <td>0</td> <td>No device connected</td> </tr> <tr> <td>1</td> <td>Device connected</td> </tr> </table> <p>(write)ClearPortEnable The HCD writes a '1' to clear the PortEnableStatus bit. Writing '0' has no effect. The CurrentConnectStatus is not affected by any write. Note: This bit is always read '1' when the attached device is nonremovable(DviceRemoveable[NumberDownstreamPort]).</p> | 0 | No device connected | 1 | Device connected |
| 0 | No device connected | | | | | | | |
| 1 | Device connected | | | | | | | |

8.4.1.5. USB_HCI Interface Control and PHY Interface Description

8.4.1.5.1. HCI Interface Control Register(Default Value: 0x10000000)

| | | | |
|---------------|-----|-------------|--|
| Offset: 0x800 | | | Register Name: HCI_ICR |
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | Reserved. |
| 28 | R | 1 | DMA Transfer Status Enable 0: Disable |

| | | | |
|-------|-----|---|--|
| | | | 1: Enable |
| 27:26 | / | / | Reserved. |
| 25 | R/W | 0 | OHCI count select 1: Simulation mode, the counters will be much shorter then real time 0: Normal mode, the counters will count full time |
| 24 | R/W | 0 | Simulation mode 1: Set PHY in a non-driving mode so the EHCI can detect device connection, this is used only for simulation 0: No effect |
| 23:21 | / | / | / |
| 20 | R/W | 0 | EHCI HS force Set 1 to this field force the ehci enter the high speed mode during bus reset. This field only valid when the bit 1 is set. |
| 19:18 | / | / | / |
| 17 | R/W | 0 | HSIC Connect detect 1 in this field enable the hsic phy to detect device connect pulse on the bus. |
| 16 | R/W | 0 | HSIC Connect Interrupt Enable Enable the HSIC connect interrupt. |
| 15:13 | / | / | / |
| 12 | R/W | 0 | PP2VBUS 1: ULPI wrapper interface will automatically set or clear DrvVbus register in ULPI PHY according to the port power status form the root hub 0: ULPI wrapper will ignore the difference between power status of root hub and ULPI PHY |
| 11 | R/W | 0 | AHB Master interface INCR16 enable 1: Use INCR16 when appropriate 0: do not use INCR16,use other enabled INCRX or unspecified length burst INCR |
| 10 | R/W | 0 | AHB Master interface INCR8 enable 1: Use INCR8 when appropriate 0: do not use INCR8,use other enabled INCRX or unspecified length burst INCR |
| 9 | R/W | 0 | AHB Master interface burst type INCR4 enable 1: Use INCR4 when appropriate 0: do not use INCR4,use other enabled INCRX or unspecified length burst INCR |
| 8 | R/W | 0 | AHB Master interface INCRX align enable 1: start INCRx burst only on burst x-align address 0: Start burst on any double word boundary Note: This bit must enable if any bit of 11:9 is enabled |
| 7:2 | / | / | Reserved |
| 1 | R/W | 0 | HSIC Phy Select 0:Select the UTMI Phy for the EHCI 1:Select the HSIC Phy for the EHCI |
| 0 | R/W | 0 | ULPI bypass enable。 1: Enable UTMI interface, disable ULPI interface 0: Enable ULPI interface, disable UTMI interface |

8.4.1.5.2. HSIC status Register(Default Value: 0x00000000)

| | |
|---------------|-----------------------------------|
| Offset: 0x804 | Register Name: HSIC_STATUS |
|---------------|-----------------------------------|

| Bit | R/W | Default/Hex | Description |
|-------|-----|-------------|---|
| 31:17 | / | / | / |
| 16 | R/W | 0 | HSIC Connect Status 1 in this field indicates a device connect pulse being detected on the bus. This field only valid when the EHCI HS force bit and the HSIC Phy Select bit is set. When the HSIC Connect Interrupt Enable is set, 1 in this bit will generate an interrupt to the system. This register is valid on HCI1. |
| 15:0 | / | / | / |

8.4.1.5.3. HSIC UTMI PHY TUNE Register(Default Value: 0x023438E4)

| Offset: 0x818 | | | Register Name: UTMI_TUNE |
|---------------|-----|-------------|---------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:26 | / | / | / |
| 25:23 | R/W | 0x04 | COMPDISTUNE |
| 22:20 | R/W | 0x03 | SQRXTUNE |
| 19 | R/W | 0x0 | TXPREEMPPULSETUNE |
| 18:16 | R/W | 0x04 | OTGTUNE |
| 15:12 | R/W | 0x03 | TXFSLSTUNE |
| 11:8 | R/W | 0x08 | TXVREFTUNE |
| 7:6 | R/W | 0x03 | TXHSXVTUNE |
| 5:4 | R/W | 0x02 | TXRISETUNE |
| 3:2 | R/W | 0x01 | TXRESTUNE |
| 1:0 | R/W | 0x0 | TXPREEMPAMPTUNE |

8.4.1.5.4. HSIC PHY CFG(Default Value: 0x00000000)

| Offset: 0x820 | | | Register Name: HSIC_CFG |
|---------------|-----|-------------|--------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:24 | / | / | / |
| 23 | R/W | 0x0 | SIDDQ |
| 22:16 | R/W | 0x0 | REF CLK |
| 15 | R/W | 0x0 | BIST EN |
| 14 | R/W | 0x0 | LOOP BACK |
| 13 | R/W | 0x0 | T OUT SEL |
| 12 | R/W | 0x0 | T CLK |
| 11:8 | R/W | 0x0 | T ADDR |
| 7:0 | R/W | 0x0 | T DATA |

8.4.1.5.5. HSIC PHY STATUS(Default Value: 0x00000000)

| Offset: 0x824 | | | Register Name: HSIC_STATUS |
|---------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:6 | / | / | / |
| 5 | R/W | 0x0 | BIST Error 0: HSIC BIST Pass 1: HSIC BIST Fail |
| 4 | R/W | 0x0 | Bist Done 0: HSIC BIST is in progress 1: HSIC BIST is done |
| 3:0 | R/W | 0x0 | T DATA OUT HSIC Test Data Out |

8.5. I2S/PCM

8.5.1. Overview

The I2S/PCM Controller has been designed to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified mode format, Right-justified mode format and PCM mode format and TDM mode format.

The I2S/PCM controller includes the following features:

- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Support different sample period width in each interface when using LRCK and LRCKR at the same time
- Support full-duplex synchronous work mode
- Support Master/Slave mode
- Support adjustable interface voltage
- Support clock up to 100MHz
- Support adjustable audio sample resolution from 8-bit to 32-bit
- Support up to 8 slots which has adjustable width from 8-bit to 32-bit
- Support sample rate from 8KHz to 192KHz
- Support 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width FIFO for data transmit, one 64 depth x 32-bit width FIFO for data receive
- Support programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA Support
- Support loopback mode for test

8.5.2. Signal Description

8.5.2.1. I2S/PCM Pin List

| Signal Name | Direction(M) | Description |
|-------------|--------------|--------------------------------|
| PCM_DIN | I | I2S/PCM Serial Data Input |
| PCM_DOUT | O | I2S/PCM Serial Data Output |
| PCM_BCLK | I/O | I2S/PCM Sample Rate Clock |
| PCM_SYNC | I/O | I2S/PCM Sample Rate Clock/Sync |

8.5.2.2. I2S/PCM Clock Source and Frequency

| | Description |
|-----------|---|
| Audio_PLL | 24.576Mhz or 22.5792Mhz generated by AUDIO-PLL to produce 48KHz or 44.1KHz serial frequency |

8.5.3. Functionalities Description

8.5.3.1. Typical Applications

The TDM is the extended of I2S and PCM which provides a serial bus interface for stereo and multichannel audio data. This interface is most commonly used by consumer audio market, including compact disc, digital audio tape, digital

sound processors, and digital TV-sound.

8.5.3.2. Functional Block Diagram

The I2S/PCM Interface block diagram is shown below:

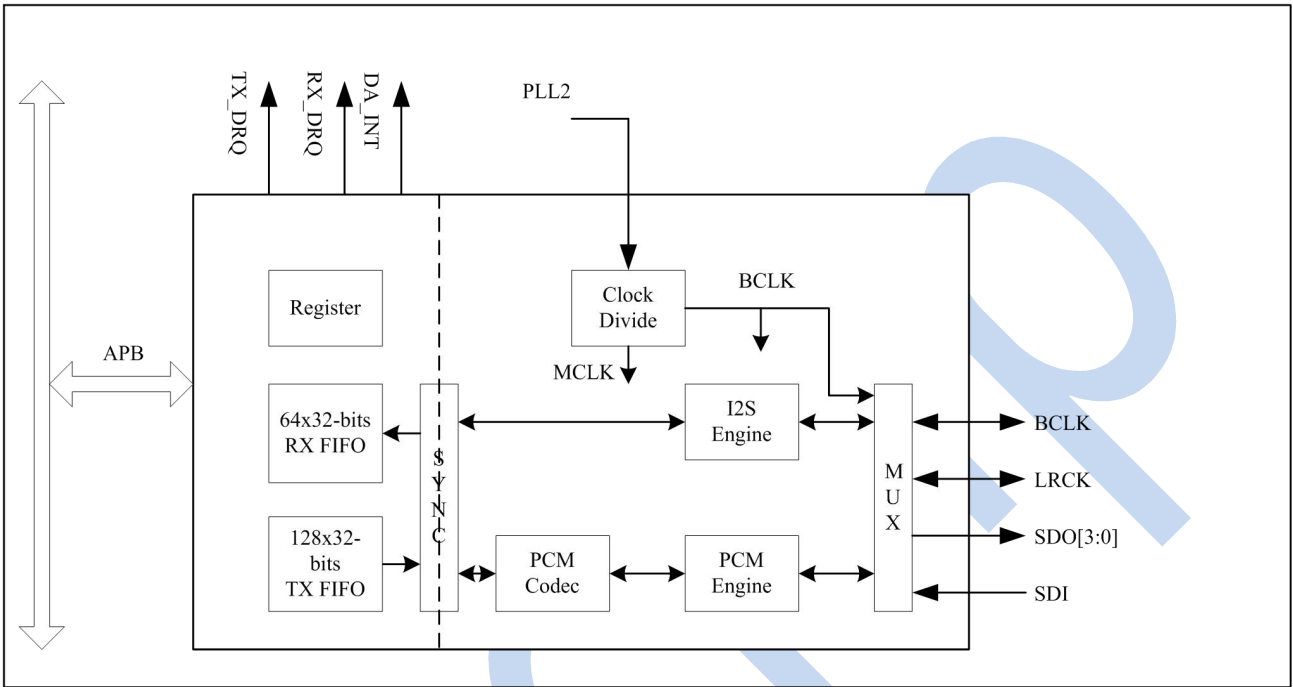


Figure 8-7. I2S/PCM Interface System Block Diagram

8.5.4. Timing Diagram

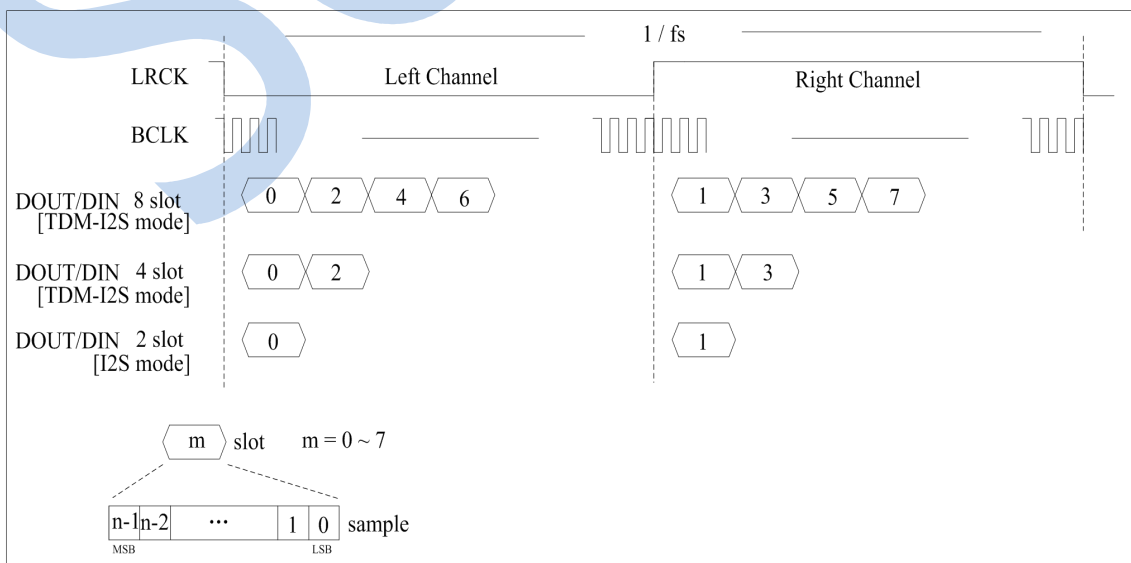


Figure 8-8. Timing Diagram for I2S/TDM-I2S Mode

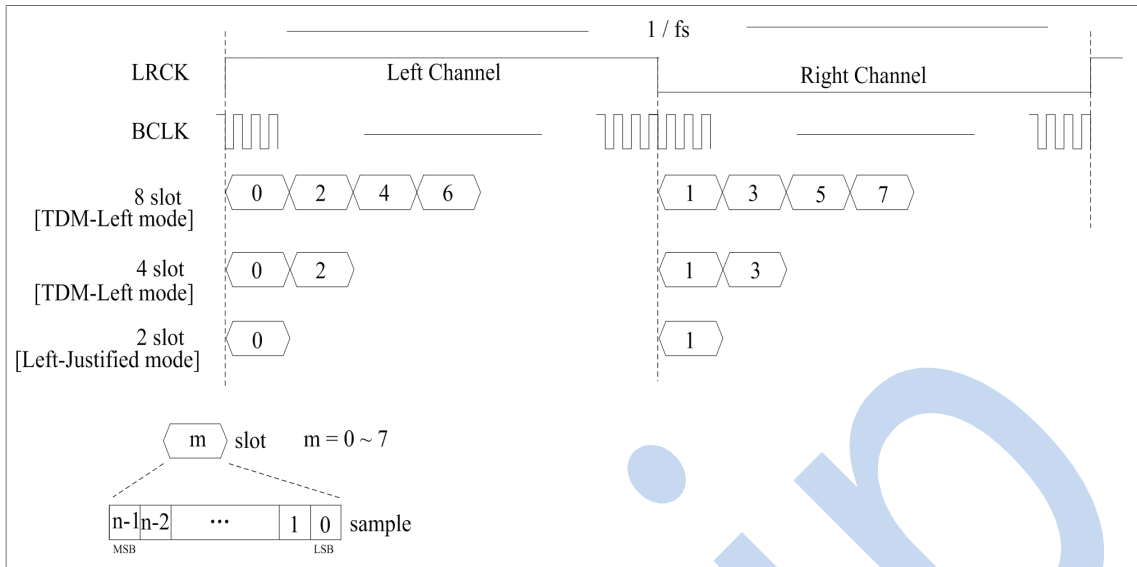


Figure 8-9. Timing Diagram for Left-justified/TDM-Left Mode

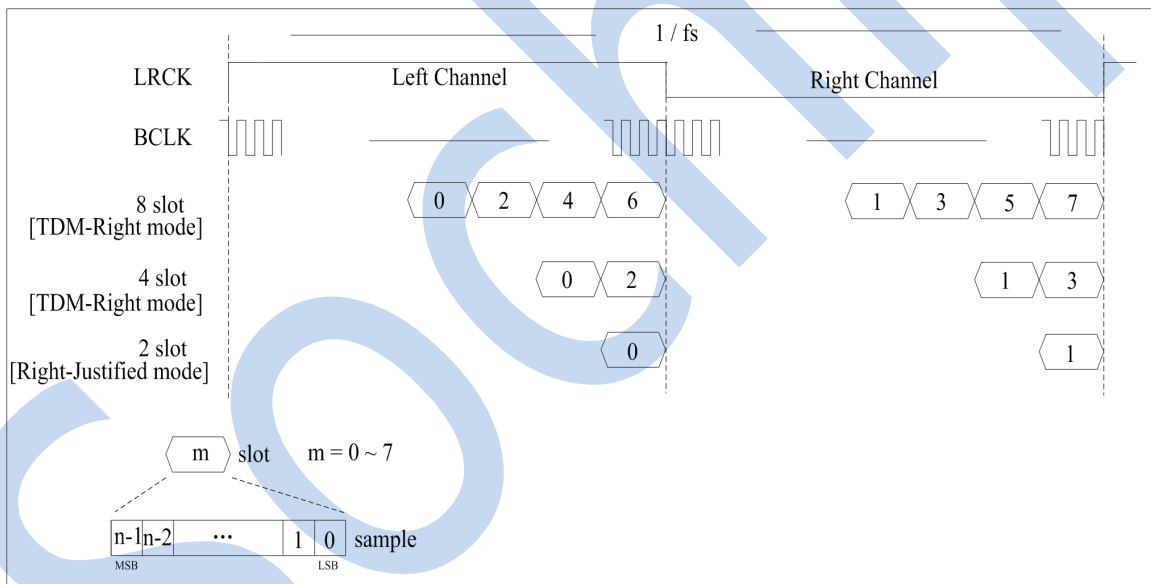


Figure 8-10. Timing Diagram for Right-justified/TDM-Right Mode



Figure 8-11. Timing Diagram for PCM/TDM-PCM Mode

8.5.5. Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup and Enable/Disable module. These five steps are described in detail in the following sections.

8.5.5.1. System setup and I2S/PCM initialization

The first step in the system setup is properly programming the GPIO. Because the I2S/PCM port is a multiplex pin. You can find the function in the pin multiplex specification. The clock source for the I2S/PCM should be followed. At first you must reset the audio PLL though the PLL_ENABLE bit of PLL_AUDIO_CTRL_REG in the CCU. The second step, you must setup the frequency of the audio pll in the PLL_AUDIO_CTRL_REG. The configuration of audio pll can be found in chapter 3. After that, you must open the I2S/PCM gating though the I2S/PCM_CLK_REG when you checkout that the LOCK bit of PLL_AUDIO_CTRL_REG become 1. At last, you must reset the I2S/PCM through the Bus Software Reset Register3's bit[12] and open the I2S/PCM bus gating in the Bus Clock Gating Register2's bit[12].

After the system setup, the register of I2S/PCM can be setup. At first, you should initialization the I2S/PCM. You should closed the globe enable bit(DA_CTL[0]), TX enable bit(DA_CTL[2]) and RX enable bit(DA_CTL[1]) by write 0 to it. After that, you must clear the TX/RX FIFO by write 0 to register DA_FCTL[25:24]. At last, you can clear the TX/RX FIFO counter by write 0 to DA_TXCNT/DA_RXCNT.

8.5.5.2. The channel setup and DMA setup

Before the usage and control of I2S/PCM, you must configure the I2C. The configuration of I2C will not describe in this chapter. But you can only configure I2S/PCM of master and slave though the I2C. In the following, you can setup the I2S/PCM of mater and slave. The configuration can be referred to the the protocol of I2S/PCM. Then, you can set the

translation mode, the sample precision, the wide of slot, the frame mode and the trigger level. The register set can be found in the spec.

The I2S/PCM support three methods to transfer the data. The most common way is DMA, the set of DMA can be found in the DMA spec. In this module, you just to enable the DRQ.

8.5.5.3. Enable and disable the I2S/PCM

To enable the function, you can enable TX/RX by write the DA_CTL[2:1]. After that, you must enable I2S/PCM by write the Globe Enable bit to 1 in the DA_CTL. The disable process is write the Globe Enable to 0.

8.5.6. I2S/PCM Interface Register List

| | |
|-------------|--------------|
| Module Name | Base Address |
| I2S/PCM | 0x01C22000 |

| Register Name | Offset | Description |
|------------------|--------|--|
| I2S/PCM_CTL | 0x00 | I2S/PCM Control Register |
| I2S/PCM_FMT0 | 0x04 | I2S/PCM Format Register 0 |
| I2S/PCM_FMT1 | 0x08 | I2S/PCM Format Register 1 |
| I2S/PCM_ISTA | 0x0C | I2S/PCM Interrupt Status Register |
| I2S/PCM_RXFIFO | 0x10 | I2S/PCM RX FIFO Register |
| I2S/PCM_FCTL | 0x14 | I2S/PCM FIFO Control Register |
| I2S/PCM_FSTA | 0x18 | I2S/PCM FIFO Status Register |
| I2S/PCM_INT | 0x1C | I2S/PCM DMA & Interrupt Control Register |
| I2S/PCM_TXFIFO | 0x20 | I2S/PCM TX FIFO Register |
| I2S/PCM_CLKD | 0x24 | I2S/PCM Clock Divide Register |
| I2S/PCM_TXCNT | 0x28 | I2S/PCM TX Sample Counter Register |
| I2S/PCM_RXCNT | 0x2C | I2S/PCM RX Sample Counter Register |
| I2S/PCM_CHCFG | 0x30 | I2S/PCM Channel Configuration register |
| I2S/PCM_TX0CHCFG | 0x34 | I2S/PCM TX0 Channel Configuration register |
| I2S/PCM_TX1CHSEL | 0x38 | I2S/PCM TX1 Channel Select Register |
| I2S/PCM_TX2CHSEL | 0x3C | I2S/PCM TX2 Channel Select Register |
| I2S/PCM_TX3CHSEL | 0x40 | I2S/PCM TX3 Channel Select Register |
| I2S/PCM_TX0CHMAP | 0x44 | I2S/PCM TX0 Channel Mapping Register |
| I2S/PCM_TX1CHMAP | 0x48 | I2S/PCM TX1 Channel Mapping Register |
| I2S/PCM_TX2CHMAP | 0x4C | I2S/PCM TX2 Channel Mapping Register |
| I2S/PCM_TX3CHMAP | 0x50 | I2S/PCM TX3 Channel Mapping Register |
| I2S/PCM_RXCHSEL | 0x54 | I2S/PCM RX Channel Select register |
| I2S/PCM_RXCHMAP | 0x58 | I2S/PCM RX Channel Mapping Register |

8.5.7. I2S/PCM Interface Register Description

8.5.7.1. I2S/PCM Control Register(Default Value: 0x00060000)

| | | | |
|--------------|-----|-------------|----------------------------|
| Offset: 0x00 | | | Register Name: I2S/PCM_CTL |
| Bit | R/W | Default/Hex | Description |

| | | | |
|-------|-----|---|--|
| 31:19 | / | / | / |
| 18 | R/W | 1 | BCLK_OUT 0: input 1: output |
| 17 | R/W | 1 | LRCK_OUT 0: input 1: output |
| 16 | R/W | 0 | LRCKR_OUT 0: input 1: output |
| 15:12 | / | / | / |
| 11 | R/W | 0 | / |
| 10 | R/W | 0 | / |
| 9 | R/W | 0 | / |
| 8 | R/W | 0 | SDO0_EN 0: Disable, Hi-Z state 1: Enable |
| 7 | / | / | / |
| 6 | R/W | 0 | OUT Mute 0: normal transfer 1: force DOUT to output 0 |
| 5:4 | R/W | 0 | MODE_SEL Mode Selection 0: PCM mode (offset 0: DSP_B; offset 1: DSP_A) 1: Left mode (offset 0: LJ mode; offset 1: I2S mode) 2: Right-Justified mode 3: Reserved |
| 3 | R/W | 0 | LOOP Loop back test 0: Normal mode 1: Loop back test When set '1', connecting the SDO0 with the SDI |
| 2 | R/W | 0 | TXEN Transmitter Block Enable 0: Disable 1: Enable |
| 1 | R/W | 0 | RXEN Receiver Block Enable 0: Disable 1: Enable |
| 0 | R/W | 0 | GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable |

8.5.7.2. I2S/PCM Format Register0 (Default Value: 0x00000033)

| Offset: 0x04 | | | Register Name: I2S/PCM_FMT0 |
|--------------|-----|-------------|------------------------------------|
| Bit | R/W | Default/Hex | Description |

| | | | |
|-------|-----|---|--|
| 31 | R/W | 0 | SDI_SYNC_SEL 0: SDI use LRCK 1: SDI use LRCKR |
| 30 | R/W | 0 | LRCK_WIDTH (only apply in PCM mode) LRCK width 0: LRCK = 1 BCLK width (short frame) 1: LRCK = 2 BCLK width (long frame) |
| 29:20 | R/W | 0 | LRCKR_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM mode: Number of BCLKs within (Left + Right) channel width I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) N+1 For example: n = 7: 8 BCLK width ... n = 1023: 1024 BCLKs width |
| 19 | R/W | 0 | LRCK_POLARITY/LRCKR_POLARITY When apply in I2S / Left-Justified / Right-Justified mode: 0: Left channel when LRCK is low 1: Left channel when LRCK is high When apply in PCM mode: 0: PCM LRCK/LRCKR asserted at the negative edge 1: PCM LRCK/LRCKR asserted at the positive edge |
| 18 | / | / | / |
| 17:8 | R/W | 0 | LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM mode: Number of BCLKs within (Left + Right) channel width I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) N+1 For example: n = 7: 8 BCLK width ... n = 1023: 1024 BCLKs width |
| 7 | R/W | 0 | BCLK_POLARITY 0: normal mode, negative edge drive and positive edge sample 1: invert mode, positive edge drive and negative edge sample |
| 6:4 | R/W | 3 | SR Sample Resolution 0: Reserved 1: 8-bit 2: 12-bit 3: 16-bit 4: 20-bit 5: 24-bit 6: 28-bit 7: 32-bit |
| 3 | R/W | 0 | EDGE_TRANSFER 0: SDO drive data and SDI sample data at the different BCLK edge 1: SDO drive data and SDI sample data at the same BCLK edge BCLK_POLARITY = 0, use negative edge |

| | | | |
|-----|-----|-----|--|
| | | | BCLK_POLARITY = 1, use positive edge |
| 2:0 | R/W | 0x3 | SW Slot Width Select 0: Reserved 1: 8-bit 2: 12-bit 3: 16-bit 4: 20-bit 5: 24-bit 6: 28-bit 7: 32-bit |

8.5.7.3. I2S/PCM Format Register1 (Default Value: 0x00000030)

| Offset: 0x08 | | | Register Name: I2S/PCM_FMT1 |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | |
| 7 | R/W | 0 | RX MLS MSB / LSB First Select 0: MSB First 1: LSB First |
| 6 | R/W | 0 | TX MLS MSB / LSB First Select 0: MSB First 1: LSB First |
| 5:4 | R/W | 3 | SEXT Sign Extend in slot [sample resolution < slot width] 0: Zeros or audio gain padding at LSB position 1: Sign extension at MSB position 2: Reserved 3: Transfer 0 after each sample in each slot |
| 3:2 | R/W | 0 | RX_PDM PCM Data Mode 0: Linear PCM 1: reserved 2: 8-bits u-law 3: 8-bits A-law |
| 1:0 | R/W | 0 | TX_PDM PCM Data Mode 0: Linear PCM 1: reserved 2: 8-bits u-law 3: 8-bits A-law |

8.5.7.4. I2S/PCM Interrupt Status Register(Default Value: 0x00000010)

| Offset: 0x0C | | | Register Name: I2S/PCM_ISTA |
|--------------|-----|-------------|-----------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:7 | / | / | / |

| | | | |
|---|-----|---|--|
| 6 | R/W | 0 | TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write 1 to clear this interrupt |
| 5 | R/W | 0 | TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt |
| 4 | R/W | 1 | TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt when data in TX FIFO are less than TX trigger level Write '1' to clear this interrupt or automatic clear if interrupt condition fails. |
| 3 | / | / | / |
| 2 | R/W | 0 | R XU_INT RX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1:FIFO Under run Pending Interrupt Write 1 to clear this interrupt |
| 1 | R/W | 0 | R XO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt |
| 0 | R/W | 0 | R XA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ when data in RX FIFO are more than RX trigger level Write '1' to clear this interrupt or automatic clear if interrupt condition fails. |

8.5.7.5. I2S/PCM RX FIFO Register(Default Value: 0x00000000)

| Offset: 0x10 | | | Register Name: I2S/PCM_RXFIFO |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample. |

8.5.7.6. I2S/PCM FIFO Control Register (Default Value: 0x000400F0)

| Offset: 0x14 | | | Register Name: I2S/PCM_FCTL |
|--------------|-----|-------------|------------------------------------|
| Bit | R/W | Default/Hex | Description |

| | | | |
|-------|-----|------|--|
| 31:26 | / | / | / |
| 25 | R/W | 0 | FTX Write '1' to flush TX FIFO, self clear to '0'. |
| 24 | R/W | 0 | FRX Write '1' to flush RX FIFO, self clear to '0'. |
| 23:19 | / | / | / |
| 18:12 | R/W | 0x40 | TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL |
| 11:10 | / | / | / |
| 9:4 | R/W | 0xF | RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1 |
| 3 | / | / | / |
| 2 | R/W | 0 | TXIM TX FIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bits transmitted audio sample: Mode 0: FIFO_I[31:0] = {APB_WDATA[31:12], 12'h0} Mode 1: FIFO_I[31:0] = {APB_WDATA[19:0], 12'h0} |
| 1:0 | R/W | 0 | RXOM RX FIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of DA_RXFIFO register. 01: Expanding received sample sign bit at MSB of DA_RXFIFO register. 10: Truncating received samples at high half-word of DA_RXFIFO register and low half-word of DA_RXFIFO register is filled by '0'. 11: Truncating received samples at low half-word of DA_RXFIFO register and high half-word of DA_RXFIFO register is expanded by its sign bit. Example for 20-bits received audio sample: Mode 0: APB_RDATA[31:0] = {FIFO_O[31:12], 12'h0} Mode 1: APB_RDATA [31:0] = {12{FIFO_O[31]}, FIFO_O[31:12]} Mode 2: APB_RDATA [31:0] = {FIFO_O[31:16], 16'h0} Mode 3: APB_RDATA [31:0] = {16{FIFO_O[31]}, FIFO_O[31:16]} |

8.5.7.7. I2S/PCM FIFO Status Register (Default Value: 0x10800000)

| Offset: 0x18 | | | Register Name: I2S/PCM_FSTA |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:29 | / | / | / |
| 28 | R | 1 | TXE TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word) |
| 27:24 | / | / | / |
| 23:16 | R | 0x80 | TXE_CNT TX FIFO Empty Space Word Counter |
| 15:9 | / | / | / |

| | | | |
|-----|---|---|---|
| 8 | R | 0 | RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word) |
| 7 | / | / | / |
| 6:0 | R | 0 | RXA_CNT RX FIFO Available Sample Word Counter |

8.5.7.8. I2S/PCM DMA & Interrupt Control Register(Default Value: 0x00000000)

| Offset: 0x1C | | | Register Name: I2S/PCM_INT |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:8 | / | / | / |
| 7 | R/W | 0 | TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable |
| 6 | R/W | 0 | TXUI_EN TX FIFO Under run Interrupt Enable 0: Disable 1: Enable |
| 5 | R/W | 0 | TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to '1', an interrupt happens when writing new audio data if TX FIFO is full. |
| 4 | R/W | 0 | TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable |
| 3 | R/W | 0 | RX_DRQ RX FIFO Data Available DRQ Enable 0: Disable 1: Enable When set to '1', RXFIFO DMA Request line is asserted if Data is available in RX FIFO. |
| 2 | R/W | 0 | RXUI_EN RX FIFO Under run Interrupt Enable 0: Disable 1: Enable |
| 1 | R/W | 0 | RXOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable |
| 0 | R/W | 0 | RXAI_EN RX FIFO Data Available Interrupt Enable 0: Disable 1: Enable |

8.5.7.9. I2S/PCM TX FIFO Register(Default Value: 0x00000000)

| Offset: 0x20 | | | Register Name: I2S/PCM_TXFIFO |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | W | 0 | TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample. |

8.5.7.10. I2S/PCM Clock Divide Register(Default Value: 0x00000000)

| Offset: 0x24 | | | Register Name: I2S/PCM_CLKD |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:9 | / | / | / |
| 8 | R/W | 0 | MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output Notes: Whether in Slave or Master mode, when this bit is set to 1, MCLK should be output. |
| 7:4 | R/W | 0 | BCLKDIV BCLK Divide Ratio from PLL2 0: reserved 1: Divide by 1 2: Divide by 2 3: Divide by 4 4: Divide by 6 5: Divide by 8 6: Divide by 12 7: Divide by 16 8: Divide by 24 9: Divide by 32 10: Divide by 48 11: Divide by 64 12: Divide by 96 13: Divide by 128 14: Divide by 176 15: Divide by 192 |
| 3:0 | R/W | 0 | MCLKDIV MCLK Divide Ratio from PLL2 Output 0: reserved 1: Divide by 1 2: Divide by 2 3: Divide by 4 4: Divide by 6 5: Divide by 8 6: Divide by 12 7: Divide by 16 8: Divide by 24 9: Divide by 32 10: Divide by 48 |

| | | | |
|--|--|--|---|
| | | | 11: Divide by 64 12: Divide by 96 13: Divide by 128 14: Divide by 176 15: Divide by 192 |
|--|--|--|---|

8.5.7.11. I2S/PCM TX Counter Register(Default Value: 0x00000000)

| Offset: 0x28 | | | Register Name: I2S/PCM_TXCNT |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. |

8.5.7.12. I2S/PCM RX Counter Register(Default Value: 0x00000000)

| Offset: 0x2C | | | Register Name: I2S/PCM_RXCNT |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. |

8.5.7.13. I2S/PCM Channel Configuration Register(Default Value: 0x00000000)

| Offset: 0x30 | | | Register Name: I2S/PCM_CHCFG |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:10 | / | / | / |
| 9 | R/W | 0 | TX_SLOT_HIZ 0: normal mode for the last half cycle of BCLK in the slot 1: turn to hi-z state for the last half cycle of BCLK in the slot |
| 8 | R/W | 0 | TXn_STATE 0: transfer level 0 when not transferring slot 1: turn to hi-z state when not transferring slot |
| 7 | / | / | / |
| 6:4 | R/W | 0 | RX_SLOT_NUM RX Channel/Slot Number which between CPU/DMA and FIFO 0: 1 channel or slot ... 7: 8 channels or slots |

| | | | |
|-----|-----|---|---|
| 3 | / | / | / |
| | | | TX_SLOT_NUM TX Channel/Slot Number which between CPU/DMA and FIFO 0: 1 channel or slot ... 7: 8 channels or slots |
| 2:0 | R/W | 0 | |

8.5.7.14. I2S/PCM TXn Channel Select Register(Default Value: 0x00000000)

| Offset: 0x34 + n*4 (n = 0, 1, 2, 3) | | | Register Name: I2S/PCM_TXnCHSEL |
|-------------------------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| 13:12 | R/W | 0 | TXn_OFFSET TXn offset tune, TXn data offset to LRCK 0: no offset n: data is offset by n BCLKs to LRCK |
| 11:4 | R/W | 0 | TXn_CHEN TXn Channel (slot) enable, bit[11:4] refer to slot [7:0]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state 0: disable 1: enable |
| 3 | / | / | / |
| | | | TXn_CHSEL TXn Channel (slot) number Select for each output 0: 1 channel / slot ... 7: 8 channels / slots |
| 2:0 | R/W | 0 | |

8.5.7.15. I2S/PCM TXn Channel Mapping Register(Default Value: 0x00000000)

| Offset: 0x44 + n*4 (n = 0, 1, 2, 3) | | | Register Name: I2S/PCM_TXnCHMAP |
|-------------------------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30:28 | R/W | 0 | TXn_CH7_MAP TXn Channel7 Mapping 0: 1st sample ... 7: 8th sample |
| 27 | / | / | / |
| 26:24 | R/W | 0 | TXn_CH6_MAP TXn Channel6 Mapping 0: 1st sample ... 7: 8th sample |
| 23 | / | / | / |
| 22:20 | R/W | 0 | TXn_CH5_MAP TXn Channel5 Mapping 0: 1st sample |

| | | | |
|-------|-----|---|--|
| | | | ... 7: 8th sample |
| 19 | / | / | / |
| 18:16 | R/W | 0 | TXn_CH4_MAP TXn Channel4 Mapping 0: 1st sample ... 7: 8th sample |
| 15 | / | / | / |
| 14:12 | R/W | 0 | TXn_CH3_MAP TXn Channel3 Mapping 0: 1st sample ... 7: 8th sample |
| 11 | / | / | / |
| 10:8 | R/W | 0 | TXn_CH2_MAP TXn Channel2 Mapping 0: 1st sample ... 7: 8th sample |
| 7 | / | / | / |
| 6:4 | R/W | 0 | TXn_CH1_MAP TXn Channel1 Mapping 0: 1st sample ... 7: 8th sample |
| 3 | / | / | / |
| 2:0 | R/W | 0 | TXn_CH0_MAP TXn Channel0 Mapping 0: 1st sample ... 7: 8th sample |

8.5.7.16. I2S/PCM RX Channel Select register(Default Value: 0x00000000)

| Offset: 0x54 | | | Register Name: I2S/PCM_RXCHSEL |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| 13:12 | R/W | 0 | RX_OFFSET RX offset tune, RX data offset to LRCK 0: no offset n: data is offset by n BCLKs to LRCK |
| 11:3 | / | / | |
| 2:0 | R/W | 0 | RX_CHSEL RX Channel (slot) number Select for input 0: 1 channel / slot ... 7: 8 channels / slots |

8.5.7.17. I2S/PCM RX Channel Mapping Register (Default Value: 0x00000000)

| Offset: 0x58 | | | Register Name: I2S/PCM_RXCHMAP |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | / | / | / |
| 30:28 | R/W | 0 | RX_CH7_MAP RX Channel7 Mapping 0: 1st sample ... 7: 8th sample |
| 27 | / | / | / |
| 26:24 | R/W | 0 | RX_CH6_MAP RX Channel6 Mapping 0: 1st sample ... 7: 8th sample |
| 23 | / | / | / |
| 22:20 | R/W | 0 | RX_CH5_MAP RX Channel5 Mapping 0: 1st sample ... 7: 8th sample |
| 19 | / | / | / |
| 18:16 | R/W | 0 | RX_CH4_MAP RX Channel4 Mapping 0: 1st sample ... 7: 8th sample |
| 15 | / | / | / |
| 14:12 | R/W | 0 | RX_CH3_MAP RX Channel3 Mapping 0: 1st sample ... 7: 8th sample |
| 11 | / | / | / |
| 10:8 | R/W | 0 | RX_CH2_MAP RX Channel2 Mapping 0: 1st sample ... 7: 8th sample |
| 7 | / | / | / |
| 6:4 | R/W | 0 | RX_CH1_MAP TX Channel1 Mapping 0: 1st sample ... 7: 8th sample |
| 3 | / | / | / |
| 2:0 | R/W | 0 | RX_CH0_MAP RX Channel0 Mapping 0: 1st sample ... |

| | | | |
|--|--|--|---------------|
| | | | 7: 8th sample |
|--|--|--|---------------|

Sochip

8.6. EMAC

8.6.1. Overview

The Ethernet MAC(EMAC) controller enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10M/100M/1000M external PHY with MII/RGMII interface in both full and half duplex mode. The internal DMA is designed for packet-oriented data transfers based on a linked list of descriptors. 4K Byte TXFIFO and 16K Byte RXFIFO are provided to keep continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are also supported in this module.

The EMAC controller includes the following features:

- Supports 10/100/1000Mbps data transfer rates
- Supports MII/RGMII PHY interface
- Supports both full-duplex and half-duplex operation
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Linked-list (chained) descriptor chaining
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- 4KB TXFIFO for transmission packets and 16KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

8.6.2. Block Diagram

The EMAC controller system block diagram is shown below:

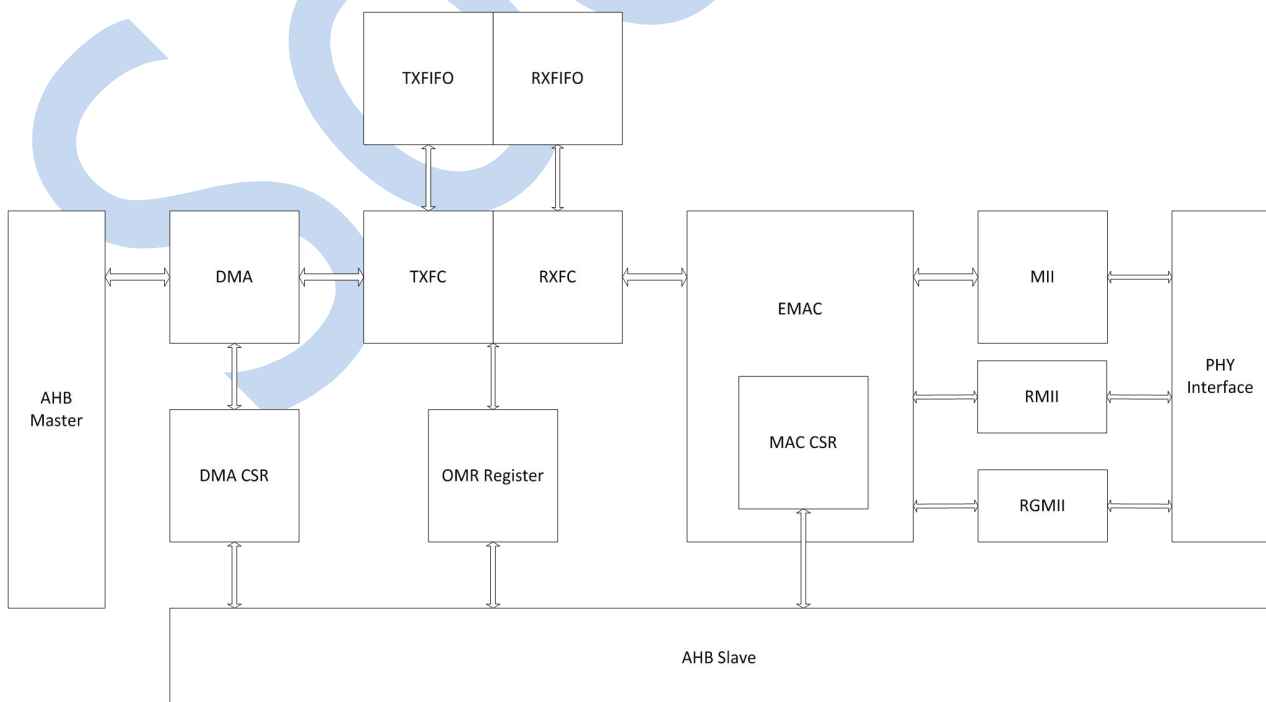


Figure7-12. EMAC Block Diagram

8.6.3. EMAC Core Register List

| Module Name | Base Address |
|-------------|--------------|
| EMAC | 0x01C30000 |

| Register Name | Offset | Description |
|------------------|----------|---|
| BASIC_CTL_0 | 0x00 | Basic Control 0 Register |
| BASIC_CTL_1 | 0x04 | Basic Control 1 Register |
| INT_STA | 0x08 | Interrupt Status Register |
| INT_EN | 0x0C | Interrupt Enable Register |
| TX_CTL_0 | 0x10 | Transmit Control 0 Register |
| TX_CTL_1 | 0x14 | Transmit Control 1 Register |
| TX_FLOW_CTL | 0x1C | Transmit Flow Control Register |
| TX_DMA_DESC_LIST | 0x20 | Transmit Descriptor List Address Register |
| RX_CTL_0 | 0x24 | Receive Control 0 Register |
| RX_CTL_1 | 0x28 | Receive Control 1 Register |
| RX_DMA_DESC_LIST | 0x34 | Receive Descriptor List Address Register |
| RX_FRM_FLT | 0x38 | Receive Frame Filter Register |
| RX_HASH_0 | 0x40 | Hash Table 0 Register |
| RX_HASH_1 | 0x44 | Hash Table 1 Register |
| MII_CMD | 0x48 | Management Interface Command Register |
| MII_DATA | 0x4C | Management Interface Data Register |
| ADDR_HIGH_0 | 0x50 | MAC Address High Register 0 |
| ADDR_LOW_0 | 0x54 | MAC Address High Register 0 |
| ADDR_HIGH_x | 0x50+8*x | MAC Address High Register x(x:1~7) |
| ADDR_LOW_x | 0x54+8*x | MAC Address Low Register x(x:1~7) |
| TX_DMA_STA | 0xB0 | Transmit DMA Status Register |
| TX_CUR_DESC | 0xB4 | Current Transmit Descriptor Register |
| TX_CUR_BUF | 0xB8 | Current Transmit Buffer Address Register |
| RX_DMA_STA | 0xC0 | Receive DMA Status Register |
| RX_CUR_DESC | 0xC4 | Current Receive Descriptor Register |
| RX_CUR_BUF | 0xC8 | Current Receive Buffer Address Register |
| RGMII_STA | 0xD0 | RGMII Status Register |

8.6.4. EMAC Core Register Description

8.6.4.1. Basic Control 0 Register(Default Value: 0x00000000)

| Offset: 0x00 | | | Register Name: BASIC_CTL_0 |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:4 | / | / | / |
| 3:2 | R/W | 0 | SPEED 00: 1000Mbps 11: 100Mbps 10: 10Mbps 01: Reserved |
| 1 | R/W | 0 | LOOPBACK 0: Disable; 1: Enable; |
| 0 | R/W | 0 | DUPLEX |

| | | | |
|--|--|--|----------------------------------|
| | | | 0: Half-duplex 1: Full-duplex |
|--|--|--|----------------------------------|

8.6.4.2. Basic Control 1 Register(Default Value: 0x08000000)

| Offset: 0x04 | | | Register Name: BASIC_CTL_1 |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:30 | / | / | / |
| 29:24 | R/W | 8 | BURST_LEN The burst length of RX and TX DMA transfer. |
| 23:2 | / | / | / |
| 1 | R/W | 0 | RX_TX_PRI 0: RX DMA and TX DMA have same priority 1: RX DMA has priority over TX DMA |
| 0 | R/W | 0 | SOFT_RST When this bit is set, soft reset all registers and logic. All clock inputs must be valid before soft rest. This bit is cleared internally when the reset operation is completed fully. Before write any register, this bit should read a 0. |

8.6.4.3. Interrupt Status Register(Default Value: 0x00000000)

| Offset: 0x08 | | | Register Name: INT_STA |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:17 | / | / | / |
| 16 | R | 0 | RGMII_LINK_STA_INT When this bit is asserted, the link status of RGMII interface is changed. |
| 15:14 | / | / | / |
| 13 | R | 0 | RX_EARLY_INT When this bit asserted, the RX DMA had filled the first data buffer of the receive frame. |
| 12 | R | 0 | RX_OVERFLOW_INT When this bit is asserted, the RX FIFO had an overflow error. |
| 11 | R | 0 | RX_TIMEOUT_INT When this bit asserted, the length of receive frame is greater than 2048 bytes(10240 when JUMBO_FRM_EN is set) |
| 10 | R | 0 | RX_DMA_STOPPED_INT When this bit asserted, the RX DMA FSM is stopped. |
| 9 | R | 0 | RX_BUF_UA_INT When this asserted, the RX DMA can't acquire next RX descriptor and RX DMA FSM is suspended. The ownership of next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume when write to DMA_RX_START bit or next receive frame is coming. |
| 8 | R | 0 | RX_INT When this bit is asserted, a frame reception is completed. The RX DMA FSM remains in the running state. |
| 7:6 | / | / | / |
| 5 | R | 0 | TX_EARLY_INT When this bit asserted , the frame is transmitted to FIFO totally. |

| | | | |
|---|---|---|---|
| 4 | R | 0 | TX_UNDERFLOW_INT When this bit is asserted, the TX FIFO had an underflow error. |
| 3 | R | 0 | TX_TIMEOUT_INT When this bit is asserted, the transmitter had been excessively active. |
| 2 | R | 0 | TX_BUF_UA_INT When this asserted, the TX DMA can not acquire next TX descriptor and TX DMA FSM is suspended. The ownership of next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when write to DMA_TX_START bit. |
| 1 | R | 0 | TX_DMA_STOPPED_INT When this bit is asserted, the TX DMA FSM is stopped. |
| 0 | R | 0 | TX_INT When this bit is asserted, a frame transmission is completed. |

8.6.4.4. Interrupt Enable Register(Default Value: 0x00000000)

| Offset: 0x0C | | | Register Name: INT_EN |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:14 | / | / | / |
| 13 | R/W | 0 | RX_EARLY_INT_EN 0: Disable early receive interrupt enable 1: Enable early receive interrupt enable |
| 12 | R/W | 0 | RX_OVERFLOW_INT_EN 0: Disable overflow interrupt 1: Enable overflow interrupt |
| 11 | R/W | 0 | RX_TIMEOUT_INT_EN 0: Disable receive timeout interrupt 1: Enable receive timeout interrupt |
| 10 | R/W | 0 | RX_DMA_STOPPED_INT_EN 0: Disable receive DMA FSM stopped interrupt 1: Enable receive DMA FSM stopped interrupt |
| 9 | R/W | 0 | RX_BUF_UA_INT_EN 0: Disable receive buffer unavailable interrupt 1: Enable receive buffer unavailable interrupt |
| 8 | R/W | 0 | RX_INT_EN 0: Disable receive interrupt 1: Enable receive interrupt |
| 7:6 | | | |
| 5 | R/W | 0 | TX_EARLY_INT_EN 0: Disable early transmit interrupt 1: Enable early transmit interrupt |
| 4 | R/W | 0 | TX_UNDERFLOW_INT_EN 0: Disable underflow interrupt 1: Enable underflow interrupt |
| 3 | R/W | 0 | TX_TIMEOUT_INT_EN 0: Disable transmit timeout interrupt 1: Enable transmit timeout interrupt |
| 2 | R/W | 0 | TX_BUF_UA_INT_EN 0: Disable transmit buffer available interrupt 1: Enable transmit buffer available interrupt |
| 1 | R/W | 0 | TX_DMA_STOPPED_INT_EN |

| | | | |
|---|-----|---|---|
| | | | 0: Disable transmit DMA FSM stopped interrupt 1: Enable transmit DMA FSM stopped interrupt |
| 0 | R/W | 0 | TX_INT_EN 0: Disable transmit interrupt 1: Enable transmit interrupt |

8.6.4.5. Transmit Control 0 Register(Default Value: 0x00000000)

| Offset: 0x10 | | | Register Name: TX_CTL_0 |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | TX_EN Enable transmitter. 0: Disable transmitter after current transmission 1: Enable |
| 30 | R/W | 0 | TX_FRM_LEN_CTL 0: Allow to transmit frames no more than 2,048 bytes (10,240 if JUMBO_FRM_EN is set) and cut off any bytes after that 1: Allow to transmit frames of up to 16,384 bytes |
| 29:0 | / | / | / |

8.6.4.6. Transmit Control 1 Register(Default Value: 0x00000000)

| Offset: 0x14 | | | Register Name: TX_CTL_1 |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | TX_DMA_START When set this bit, the TX DMA FSM will go no to work. It is cleared internally and always read a 0. |
| 30 | R/W | 0 | TX_DMA_EN 0: Stop TX DMA after the completion of current frame transmission. 1: Start and run TX DMA. |
| 29:11 | / | / | / |
| 10:8 | R/W | 0 | TX_TH The threshold value of TX DMA FIFO. When TX_MD is 0, transmission starts when the size of frame in TX DMA FIFO is greater than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved |
| 7:2 | / | / | / |
| 1 | R/W | 0 | TX_MD 0: Transmission starts after the number of data in TX DAM FIFO is greater than TX_TH 1: Transmission starts after a full frame located in TX DMA FIFO |
| 0 | R/W | 0 | FLUSH_TX_FIFO The functionality that flush the data in the TX FIFO. 0: Enable |

| | | | |
|--|--|--|------------|
| | | | 1: Disable |
|--|--|--|------------|

8.6.4.7. Transmit Flow Control Register(Default Value: 0x00000000)

| Offset: 0x1C | | | Register Name: TX_FLOW_CTL |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After completion of transmission, this bit will be cleared automatically. Before write register TX_FLOW_CTRL, this bit must be read as 0. |
| 30:22 | / | / | / |
| 21:20 | R/W | 0 | TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic retransmission of pause frame. The threshold values should be always less than the PAUSE_TIME |
| 19:4 | R/W | 0 | PAUSE_TIME The pause time field in the transmitted control frame. |
| 3:2 | / | / | / |
| 1 | R/W | 0 | ZQP_FRM_EN When set, enable the functionality to generate Zero-Quanta Pause control frame. |
| 0 | R/W | 0 | TX_FLOW_CTL_EN When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode. 0: Disable 1: Enable |

8.6.4.8. Transmit DMA Descriptor List Address Register(Default Value: 0x00000000)

| Offset: 0x20 | | | Register Name: TX_DMA_LIST |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | TX_DESC_LIST The base address of transmit descriptor list. It must be 32-bit aligned. |

8.6.4.9. Receive Control 0 Register(Default Value: 0x00000000)

| Offset: 0x24 | | | Register Name: RX_CTL_0 |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | RX_EN Enable receiver 0: Disable receiver after current reception 1: Enable |
| 30 | R/W | 0 | RX_FRM_LEN_CTL 0: Allow to receive frames less than or equal to 2,048 bytes (10,240 if |

| | | | |
|-------|-----|---|---|
| | | | JUMBO_FRM_EN is set) and cuts off any bytes received after that 1: Allow to receive frames of up to 16,384 bytes |
| 29 | R/W | 0 | JUMBO_FRM_EN When set, allows Jumbo frames of 9,018 bytes without reporting a giant frame error in the receive frame status. |
| 28 | R/W | 0 | STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length's field value is less than or equal to 1,500 bytes. |
| 27 | R/W | 0 | CHECK_CRC When set, calculate CRC and check the IPv4 Header Checksum. |
| 26:18 | / | / | / |
| 17 | R/W | 0 | RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x standard, also detect unicast pause frame with address specified in MAC Address 0 High Register and MAC address 0 Low Register. |
| 16 | R/W | 0 | RX_FLOW_CTL_EN When set, enable the functionality that decode the received pause frame and disable its transmitter for a specified time by pause frame. |
| 15:0 | / | / | / |

8.6.4.10. Receive Control 1 Register(Default Value: 0x00000000)

| Offset: 0x28 | | | Register Name: RX_CTL_1 |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | RX_DMA_START When set, the RX DMA will go no to work. It is cleared internally and always read a 0. |
| 30 | R/W | 0 | RX_DMA_EN 0: Stop RX DMA after finish receiving current frame 1: Start and run RX DMA |
| 29:25 | / | / | / |
| 24 | R/W | 0 | RX_FIFO_FLOW_CTL 0: Disable RX flow control 1: Enable RX flow control based on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT |
| 23:22 | R/W | 0 | RX_FLOW_CTL_TH_DEACT The threshold for deactivating flow control in both half-duplex mode and full-duplex mode 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB |
| 21:20 | R/W | 0 | RX_FLOW_CTL_TH_ACT The threshold for activating flow control in both half-duplex mode and full-duplex mode. 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB |
| 19:6 | / | / | / |

| | | | |
|-----|-----|---|---|
| 5:4 | R/W | 0 | <p>RX_TH</p> <p>The threshold value of RX DMA FIFO. When RX_MD is 0, RX DMA starts to transfer data when the size of received frame in RX DMA FIFO is greater than the threshold. In addition, full frames with a length less than the threshold are transferred automatically.</p> <p>00: 64 01: 32 10: 96 11: 128</p> |
| 3 | R/W | 0 | <p>RX_ERR_FRM</p> <p>0: RX DMA drops frames with error 1: RX DMA forwards frames with error</p> |
| 2 | R/W | 0 | <p>RX_RUNT_FRM</p> <p>When set, forward undersized frames with no error and length less than 64bytes</p> |
| 1 | R/W | 0 | <p>RX_MD</p> <p>0: RX DMA reads data from RX DMA FIFO to host memory after the number of data in RX DAM FIFO is greater than RX_TH 1: RX DMA reads data from RX DMA FIFO to host memory after a complete frame has been written to RX DMA FIFO</p> |
| 0 | R/W | 0 | <p>FLUSH_RX_FRM</p> <p>The functionality that flush the frames when receive descriptors/buffers is unavailable</p> <p>0: Enable 1: Disable</p> |

8.6.4.11. Receive DMA Descriptor List Address Register(Default Value: 0x00000000)

| Offset: 0x34 | | | Register Name: RX_DMA_LIST |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | <p>RX_DESC_LIST</p> <p>The base address of receive descriptor list. It must be 32-bit aligned.</p> |

8.6.4.12. Receive Frame Filter Register(Default Value: 0x00000000)

| Offset: 0x38 | | | Register Name: RX_FRM_FLT |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | <p>DIS_ADDR_FILTER</p> <p>0: Enable address filter 1: Disable address filter</p> |
| 30:18 | / | / | / |
| 17 | R/W | 0 | <p>DIS_BROADCAST</p> <p>0: Receive all broadcast frames 1: Drop all broadcast frames</p> |
| 16 | R/W | 0 | <p>RX_ALL_MULTICAST</p> <p>0: Filter multicast frame according to HASH_MULTICAST 1: Receive all multicast frames</p> |
| 15:14 | / | / | |
| 13:12 | R/W | 0 | <p>CTL_FRM_FILTER</p> |

| | | | |
|-------|-----|---|--|
| | | | 00, 01: Drop all control frames 10: Receive all control frames 11: Receive all control frames when pass the address filter |
| 11:10 | / | / | / |
| 9 | R/W | 0 | HASH_MULTICAST 0: Filter multicast frames by comparing the DA field with the values in DA MAC address registers 1: Filter multicast frames according to the hash table |
| 8 | R/W | 0 | HASH_UNICAST 0: Filter unicast frames by comparing the DA field with the values in DA MAC address registers 1: Filter unicast frames according to the hash table |
| 7 | / | / | / |
| 6 | R/W | 0 | SA_FILTER_EN 0: Receive frames and update the result of SA filter 1: Update the result of SA filter. In addition, if the SA field of received frame does not match the values in SA MAC address registers, drop this frame. |
| 5 | R/W | 0 | SA_INV_FILTER 0: When the SA field of current frame matches the values in SA MAC address registers, it passes the SA filter 1: When the SA field of current frame does not match the values in SA MAC address registers, it passes the SA filter |
| 4 | R/W | 0 | DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode |
| 3:2 | / | / | / |
| 1 | R/W | 0 | FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter 1: Receive the frame when it pass the address register filter or the hash filter(set by HASH_MULTICAST or HASH_UNICAST) |
| 0 | R/W | 0 | RX_ALL 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter(pass or fail) in the receive status word |

8.6.4.13. Receive Hash Table 0 Register(Default Value: 0x00000000)

| Offset: 0x40 | | | Register Name: RX_HASH_0 |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | HASH_TAB_0 The upper 32 bits of Hash table for receive frame filter. |

8.6.4.14. Receive Hash Table 1 Register(Default Value: 0x00000000)

| Offset: 0x44 | | | Register Name: RX_HASH_1 |
|--------------|-----|-------------|---------------------------------|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0 | HASH_TAB_1 |

| | | | |
|--|--|--|---|
| | | | The lower 32 bits of Hash table for receive frame filter. |
|--|--|--|---|

8.6.4.15. MII Command Register(Default Value: 0x00000000)

| Offset: 0x48 | | | Register Name: MII_CMD |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:23 | / | / | / |
| 22:20 | R/W | 0 | MDC_DIV_RATIO_M MDC clock divide ration(m). The source of MDC clock is AHB clock. 000: 16 001: 32 010: 64 011: 128 Others: Reserved |
| 19:17 | / | / | / |
| 16:12 | R/W | 0 | PHY_ADDR Select a PHY device from 32 possible candidates. |
| 11:9 | / | / | / |
| 8:4 | R/W | 0 | PHY_REG_ADDR Select register in the selected PHY device |
| 3:2 | / | / | / |
| 1 | R/W | 0 | MII_WR 0: Read register in selected PHY and return data in EMAC_GMII_DATA 1: Write register in selected PHY using data in EMAC_GMII_DATA |
| 0 | R/W | 0 | MII_BUSY This bit indicates that a read or write operation is in progress. When prepared the data and register address for a write operation or the register address for a read operation, set this bit and start to access register in PHY. When this bit is cleared automatically, the read or write operation is over and the data in EMAC_GMII_DATA is valid for a read operation. |

8.6.4.16. MII Data Register(Default Value: 0x00000000)

| Offset: 0x4C | | | Register Name: MII_DATA |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | / | / | / |
| 15:0 | R/W | 0 | MII_DATA The 16-bit data to be written to or read from the register in the selected PHY. |

8.6.4.17. MAC Address 0 High Register(Default Value: 0x0000FFFF)

| Offset: 0x50 | | | Register Name: ADDR0_HIGH |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:16 | / | / | / |
| 15:0 | R/W | 0xFFFF | MAC_ADDR_0_HIGH The upper 16bits of the 1 st MAC address. |

8.6.4.18. MAC Address 0 Low Register(Default Value: 0xFFFFFFFF)

| Offset: 0x54 | | | Register Name: ADDR0_LOW |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0xFFFFFFFF | MAC_ADDR_0_LOW The lower 32bits of 1 st MAC address. |

8.6.4.19. MAC Address x High Register(Default Value: 0x0000FFFF)

| Offset: 0x50+8*x (x=1~7) | | | Register Name: ADDRx_HIGH |
|--------------------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31 | R/W | 0 | MAC_ADDR_CTL 0: MAC address x(x: 1~7) is not valid, and it will be ignored by the address filter 1: MAC address x(x : 1~7) is valid |
| 30 | R/W | 0. | MAC_ADDR_TYPE 1: MAC address x(x:1~7) used to compare with the source address of the received frame 0: MAC address x(x:1~7) used to compare with the destination address of the received frame |
| 29:24 | R/W | 0 | MAC_ADDR_BYTE_CTL MAC address byte control mask. The lower bit of mask controls the lower byte of in MAC address x(x:1~7). When the bit of mask is 1, do not compare the corresponding byte. |
| 23:16 | / | / | / |
| 15:0 | R/W | 0xFFFF | MAC_ADDR_x_HIGH The upper 16bits of the MAC address x(x:1~7). |

8.6.4.20. MAC Address x Low Register(Default Value: 0xFFFFFFFF)

| Offset: 0x54+8*x (x=1~7) | | | Register Name: ADDRx_LOW |
|--------------------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R/W | 0xFFFFFFFF | MAC_ADDR_x_LOW The lower 32bits of MAC address x(x:1~7). |

8.6.4.21. Transmit DMA Status Register(Default Value: 0x00000000)

| Offset: 0xB0 | | | Register Name: TX_DMA_STA |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:3 | / | / | / |
| 2:0 | R | 0 | TX_DMA_STA The state of Transmit DMA FSM. 000: STOP: When reset or disable TX DMA; 001: RUN_FETCH_DESC: Fetching TX DMA descriptor; 010: RUN_WAIT_STA: Waiting for the status of TX frame; 011: RUN_TRANS_DATA: Passing frame from host memory to TX DMA FIFO; 111: RUN_CLOSE_DESC: Closing TX descriptor. 110: SUSPEND: TX descriptor unavailable or TX DMA FIFO underflow; |

| | | | |
|--|--|--|---------------------|
| | | | 100, 101: Reserved; |
|--|--|--|---------------------|

8.6.4.22. Transmit DMA Current Descriptor Register(Default Value: 0x00000000)

| Offset: 0xB4 | | | Register Name: TX_DMA_CUR_DESC |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | The address of current transmit descriptor. |

8.6.4.23. Transmit DMA Current Buffer Address Register(Default Value: 0x00000000)

| Offset: 0xB8 | | | Register Name: TX_DMA_CUR_BUF |
|--------------|-----|-------------|--|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | The address of current transmit DMA buffer |

8.6.4.24. Receive DMA Status Register(Default Value: 0x00000000)

| Offset: 0xC0 | | | Register Name: RX_DMA_STA |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:3 | / | / | / |
| 2:0 | R | 0 | RX_DMA_STA The state of RX DMA FSM. 000: STOP: When reset or disable RX DMA; 001: RUN_FETCH_DESC: Fetching RX DMA descriptor; 011: RUN_WAIT_FRM: Waiting for frame. 100: SUSPEND: RX descriptor unavailable; 101: RUN_CLOSE_DESC: Closing RX descriptor. 111: RUN_TRANS_DATA: Passing frame from host memory to RX DMA FIFO; 010, 110: Reserved. |

8.6.4.25. Receive DMA Current Descriptor Register(Default Value: 0x00000000)

| Offset: 0xC4 | | | Register Name: RX_DMA_CUR_DESC |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | The address of current receive descriptor |

8.6.4.26. Receive DMA Current Buffer Address Register(Default Value: 0x00000000)

| Offset: 0xC8 | | | Register Name: RX_DMA_CUR_BUF |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:0 | R | 0 | The address of current receive DMA buffer |

8.6.4.27. RGMII Status Register(Default Value: 0x00000000)

| Offset: 0xD0 | | | Register Name: RGMII_STA |
|--------------|-----|-------------|---|
| Bit | R/W | Default/Hex | Description |
| 31:4 | / | / | / |
| 3 | R | 0 | RGMII_LINK The link status of RGMII interface 0: down 1: up |
| 2:1 | R | 0 | RGMII_LINK_SPD The link speed of RGMII interface 00: 2.5 MHz 01: 25 MHz 10: 125 MHz |
| 0 | R | 0 | RGMII_LINK_MD The link Mode of RGMII interface 0: Half-Duplex 1: Full-Duplex |

8.6.5. EMAC RX/TX Descriptor

The EMAC' internal DMA transfers data between host memory and internal RX/TX FIFO with a linked list of descriptors. Each descriptor is consisted of four words, and contains some necessary information to transfer TX and RX frames. The descriptor list structure is shown in figure 8-12. The address of each descriptor must be 32-bit aligned.

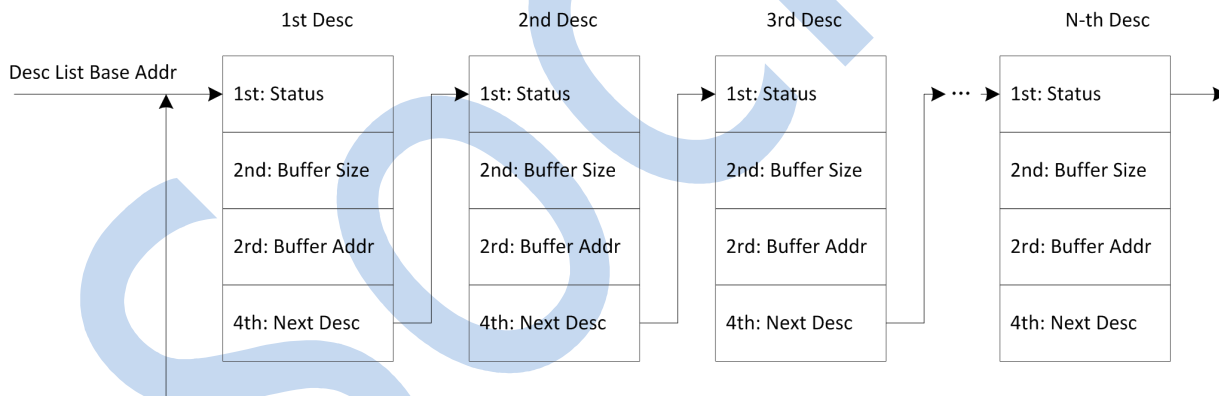


Figure 8-12. EMAC RX/TX Descriptor List

8.6.5.1. Transmit Descriptor

1st Word of Transmit Descriptor

| Bits | Description |
|-------|--|
| 31 | TX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all data in current descriptor's buffer are transmitted. |
| 30:17 | Reserved |
| 16 | TX_HEADER_ERR |

| | |
|-----|--|
| | When set, the checksum of transmitted frame's header is wrong. |
| 15 | Reserved |
| 14 | TX_LENHT_ERR When set, the length of transmitted frame is wrong. |
| 13 | Reserved |
| 12 | TX_PAYLOAD_ERR When set, the checksum of transmitted frame's payload is wrong. |
| 11 | Reserved |
| 10 | TX_CRD_ERR When set, carrier is lost during transmission. |
| 9 | TX_COL_ERR_0 When set, the frame is aborted because of collision after contention period. |
| 8 | TX_COL_ERR_1 When set, the frame is aborted because of too many collisions. |
| 7 | Reserved. |
| 6:3 | TX_COL_CNT The number of collisions before transmission. |
| 2 | TX_DEFER_ERR When set, the frame is aborted because of too much deferral. |
| 1 | TX_UNDERFLOW_ERR When set, the frame is aborted because of TX FIFO underflow error. |
| 0 | TX_DEFER When set in Half-Duplex mode, the EMAC defers the frame transmission. |

2nd Word of Transmit Descriptor

| Bits | Description |
|-------|--|
| 31 | TX_INT_CTL When set and the current frame have been transmitted, the TX_INT in Interrupt Status Register will be set. |
| 30 | LAST_DESC When set, current descriptor is the last one for current frame. |
| 29 | FIR_DESC When set, current descriptor is the first one for current frame. |
| 28:27 | CHECKSUM_CTL These bits control to insert checksums in transmit frame. |
| 26 | CRC_CTL When set, CRC field is not transmitted. |
| 25:11 | Reserved |
| 10:0 | BUF_SIZE The size of buffer specified by current descriptor. |

3rd Word of Transmit Descriptor

| Bits | Description |
|------|--|
| 31:0 | BUF_ADDR The address of buffer specified by current descriptor. |

4th Word of Transmit Descriptor

| Bits | Description |
|------|--|
| 31:0 | NEXT_DESC_ADDR The address of next descriptor. It must be 32-bit aligned. |

8.6.5.2. Receive Descriptor

1st Word of Receive Descriptor

| Bits | Description |
|-------|--|
| 31 | RX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when complete frame is received or current descriptor's buffer is full. |
| 30 | RX_DAF_FAIL When set, current frame don't pass DA filter. |
| 29:16 | RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of receive frame. |
| 15 | Reserved |
| 14 | RX_NO_ENOUGH_BUF_ERR When set, current frame is clipped because of no enough buffer. |
| 13 | RX_SAF_FAIL When set, current fame don't pass SA filter. |
| 12 | Reserved. |
| 11 | RX_OVERFLOW_ERR When set, a buffer overflow error occurred and current frame is wrong. |
| 10 | Reserved |
| 9 | FIR_DESC When set, current descriptor is the first descriptor for current frame. |
| 8 | LAST_DESC When set, current descriptor is the last descriptor for current frame. |
| 7 | RX_HEADER_ERR When set, the checksum of frame's header is wrong. |
| 6 | RX_COL_ERR When set, there is a late collision during reception in half-duplex mode. |
| 5 | Reserved. |
| 4 | RX_LENGTH_ERR When set, the length of current frame is wrong. |
| 3 | RX_PHY_ERR When set, the receive error signal from PHY is asserted during reception. |
| 2 | Reserved. |
| 1 | RX_CRC_ERR When set, the CRC filed of received frame is wrong. |
| 0 | RX_PAYLOAD_ERR When set, the checksum or length of received frame's payload is wrong. |

2nd Word of Receive Descriptor

| Bits | Description |
|-------|--|
| 31 | RX_INT_CTL When set and a frame have been received, the RX_INT will not be set. |
| 30:11 | Reserved |
| 10:0 | BUF_SIZE The size of buffer specified by current descriptor. |

3rd Word of Receive Descriptor

| Bits | Description |
|------|--|
| 31:0 | BUF_ADDR The address of buffer specified by current descriptor. |

4th Word of Receive Descriptor

| Bits | Description |
|------|--|
| 31:0 | NEXT_DESC_ADDR The address of next descriptor. This field must be 32-bit aligned. |

Chapter 9 Electrical Characteristics

9.1. Absolute Maximum Ratings

Table 9-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices.



CAUTION

- Absolute Maximum Ratings are those values beyond which damage to the device may occur.
- Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may damage to the device.

Table 9-1. Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Unit |
|-----------|-------------------------------------|------|------|------|
| $I_{I/O}$ | In/Out Current for Input and Output | -40 | 40 | mA |
| AVCC | Power Supply for Analog Part | -0.3 | 3.6 | V |
| EPHY_VCC | Power Supply for EPHY High Voltage | -0.3 | 3.63 | V |
| EPHY_VDD | Power Supply for EPHY Low Voltage | -0.3 | 1.4 | V |
| HPVCCIN | Power Supply for Headphone | -0.3 | 3.63 | V |
| VCC-IO | Power Supply for Port B,C,F,G | -0.3 | 3.63 | V |
| VCC-PD | Power Supply for Port D | -0.3 | 3.63 | V |
| VCC-PE | Power Supply for Port E | -0.3 | 3.63 | V |
| VCC-PLL | Power Supply for System PLL | -0.3 | 3.63 | V |
| VCC-MCSI | Power Supply for MIPI CSI | -0.3 | 3.63 | V |
| VCC-RTC | Power Supply for RTC | -0.3 | 3.63 | V |
| VCC-USB | Power Supply for USB | -0.3 | 3.63 | V |
| VDD-EFUSE | Power Supply for EFUSE | -0.3 | 2.75 | V |
| VCC-DRAM | Power Supply for DRAM(DDR3) | -0.3 | 1.98 | V |
| VDD-CPU | Power Supply for CPU | -0.3 | 1.4 | V |
| VDD-SYS | Power Supply for System | -0.3 | 1.4 | V |
| T_{STG} | Storage Temperature | -40 | 125 | °C |

9.2. Recommended Operating Conditions

All S3 modules are used under the operating conditions contained in Table 9-2.

Table 9-2. Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|------------------------------------|-------|-----|-------|------|
| Ta | Ambient Operating Temperature | -20 | - | +70 | °C |
| AVCC | Power Supply for Analog Part | 2.94 | 3.0 | 3.06 | V |
| EPHY_VCC | Power Supply for EPHY High Voltage | 3.0 | 3.3 | 3.6 | V |
| EPHY_VDD | Power Supply for EPHY Low Voltage | 1.0 | 1.1 | 1.2 | V |
| HPVCCIN | Power Supply for Headphone | 3.1 | 3.3 | 3.5 | V |
| VCC-IO | Power Supply for Port B,C,F,G | 2.97 | 3.3 | 3.63 | V |
| VCC-PD | Power Supply for Port D | 2.25 | 2.5 | 2.75 | V |
| | 2.5V Voltage | 2.97 | 3.3 | 3.63 | |
| | 3.3V Voltage | | | | |
| VCC-PE | Power Supply for Port E | 1.62 | 1.8 | 1.98 | V |
| | 1.8V Voltage | 2.52 | 2.8 | 3.08 | |
| | 2.8V Voltage | 2.97 | 3.3 | 3.63 | |
| | 3.3V Voltage | | | | |
| VCC-PLL | Power Supply for System PLL | 2.9 | 3.3 | 3.6 | V |
| VCC-MCSI | Power Supply for MIPI CSI | 2.97 | 3.3 | 3.63 | V |
| VCC-RTC | Power Supply for RTC | 2.97 | 3.3 | 3.63 | V |
| VCC-USB | Power Supply for USB | 3.07 | 3.3 | 3.63 | V |
| VDD-EFUSE | Power Supply for EFUSE | 2.25 | 2.5 | 2.75 | V |
| VCC-DRAM | Power Supply for DRAM(DDR3) | 1.425 | 1.5 | 1.575 | V |
| VDD-CPU | Power Supply for CPU | 1.04 | - | 1.3 | V |
| VDD-SYS | Power Supply for System | 0.99 | 1.1 | 1.21 | V |

9.3. DC Electrical Characteristics

Table 9-3 summarizes the DC electrical characteristics of S3.

Table 9-3. DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|----------------------------------|--------------|-----|--------------|------|
| VIH | High-Level Input Voltage | 0.7 * VCC-IO | - | VCC-IO + 0.3 | V |
| VIL | Low-Level Input Voltage | -0.3 | - | 0.3 * VCC-IO | V |
| RPU | Input Pull-Up Resistance | 50 | 100 | 150 | KΩ |
| RPD | Input Pull-Down Resistance | 50 | 100 | 150 | KΩ |
| IIH | High-Level Input Current | - | - | 10 | uA |
| IIL | Low-Level Input Current | - | - | 10 | uA |
| VOH | High-Level Output Voltage | VCC-IO -0.2 | - | VCC-IO | V |
| VOL | Low-Level Output Voltage | 0 | - | 0.2 | V |
| IOZ | Tri-State Output Leakage Current | -10 | - | 10 | uA |
| CIN | Input Capacitance | - | - | 5 | pF |
| COUT | Output Capacitance | - | - | 5 | pF |

9.4. Oscillator Electrical Characteristics

The S3 contains two external input clocks: X24MIN and X32KIN, two output clocks: X24MOUT and X32KOUT.

The 24MHz frequency is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through X24MIN. Table 9-4 lists the 24MHz crystal specifications.

Table 9-4. 24MHz Oscillator Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|---------------------------------------|-------------|--------|-----|------------|
| $1/(t_{CPMAIN})$ | Crystal Oscillator Frequency Range | – | 24.000 | – | MHz |
| t_{ST} | Startup Time | – | – | – | ms |
| | Frequency Tolerance at 25 °C | -50 | – | +50 | ppm |
| | Oscillation Mode | Fundamental | | | – |
| | Maximum change over temperature range | -50 | – | +50 | ppm |
| P_{ON} | Drive level | – | – | 300 | uW |
| C_L | Equivalent Load capacitance | 12 | 18 | 22 | pF |
| R_S | Series Resistance(ESR) | – | 25 | – | Ω |
| | Duty Cycle | 30 | 50 | 70 | % |
| C_M | Motional capacitance | – | – | – | pF |
| C_{SHUT} | Shunt capacitance | 5 | 6.5 | 7.5 | pF |
| R_{BIAS} | Internal bias resistor | 0.4 | 0.5 | 0.6 | M Ω |

The 32768Hz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. The clock is provided through X32KIN. Table 9-5 lists the 32768Hz crystal specifications.

Table 9-5. 32768Hz Oscillator Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|---------------------------------------|-------------|-------|-----|------------|
| $1/(t_{CPMAIN})$ | Crystal Oscillator Frequency Range | – | 32768 | – | Hz |
| t_{ST} | Startup Time | – | – | – | ms |
| | Frequency Tolerance at 25 °C | -40 | – | +40 | ppm |
| | Oscillation Mode | Fundamental | | | – |
| | Maximum Change Over Temperature Range | -50 | – | +50 | ppm |
| P_{ON} | Drive Level | – | – | 50 | uW |
| C_L | Equivalent Load Capacitance | – | – | – | pF |
| R_S | Series Resistance(ESR) | – | – | – | Ω |
| | Duty Cycle | 30 | 50 | 70 | % |
| C_M | Motional Capacitance | – | – | – | pF |
| C_{SHUT} | Shunt Capacitance | – | – | – | pF |
| R_{BIAS} | Internal Bias Resistor | – | – | – | M Ω |

9.5. Power on and Power off Sequence

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operations. Following figure 9-1 and 9-2 provides the timing requirements for the S3 power.

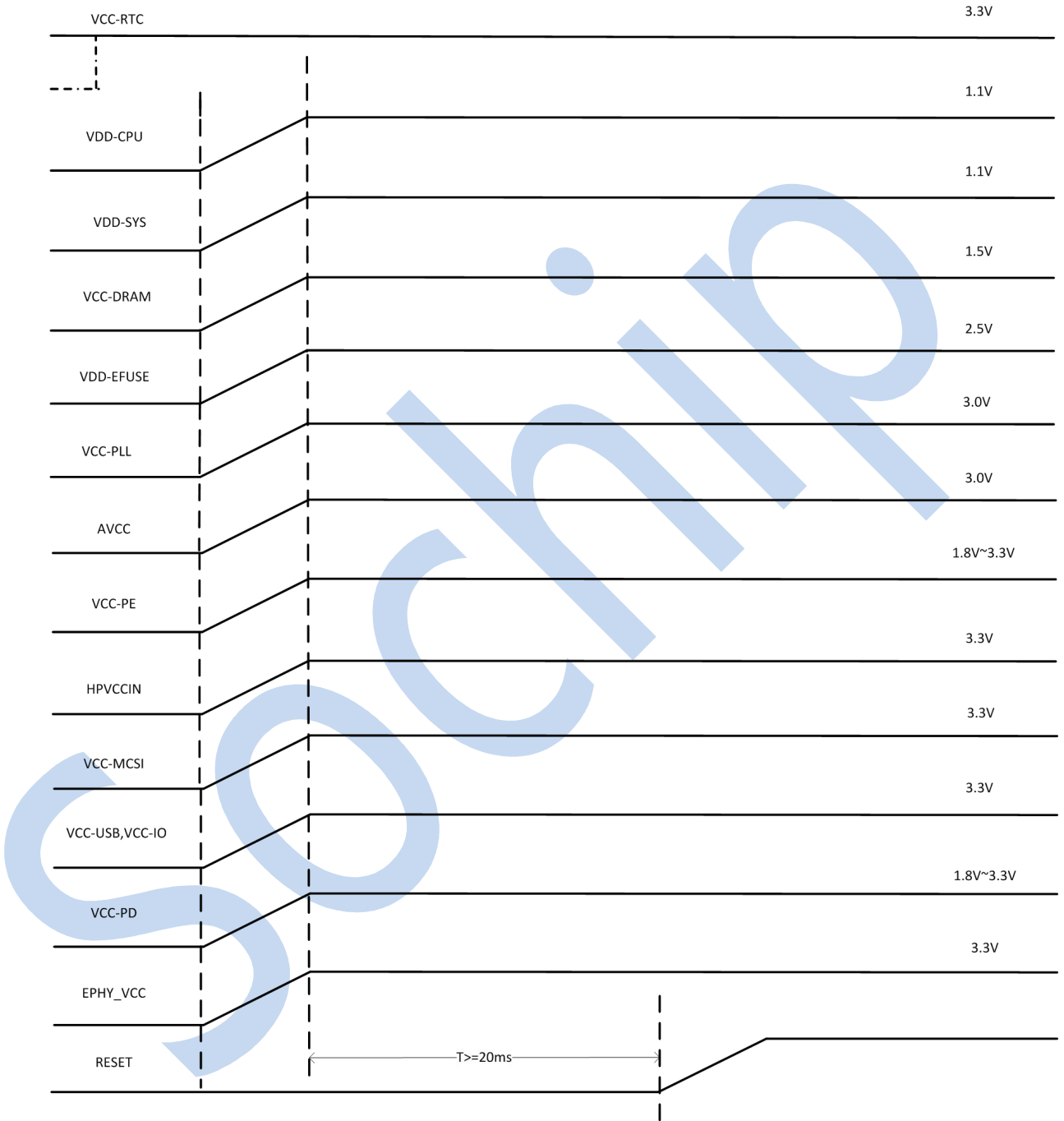


Figure 9-1. Power On Sequence

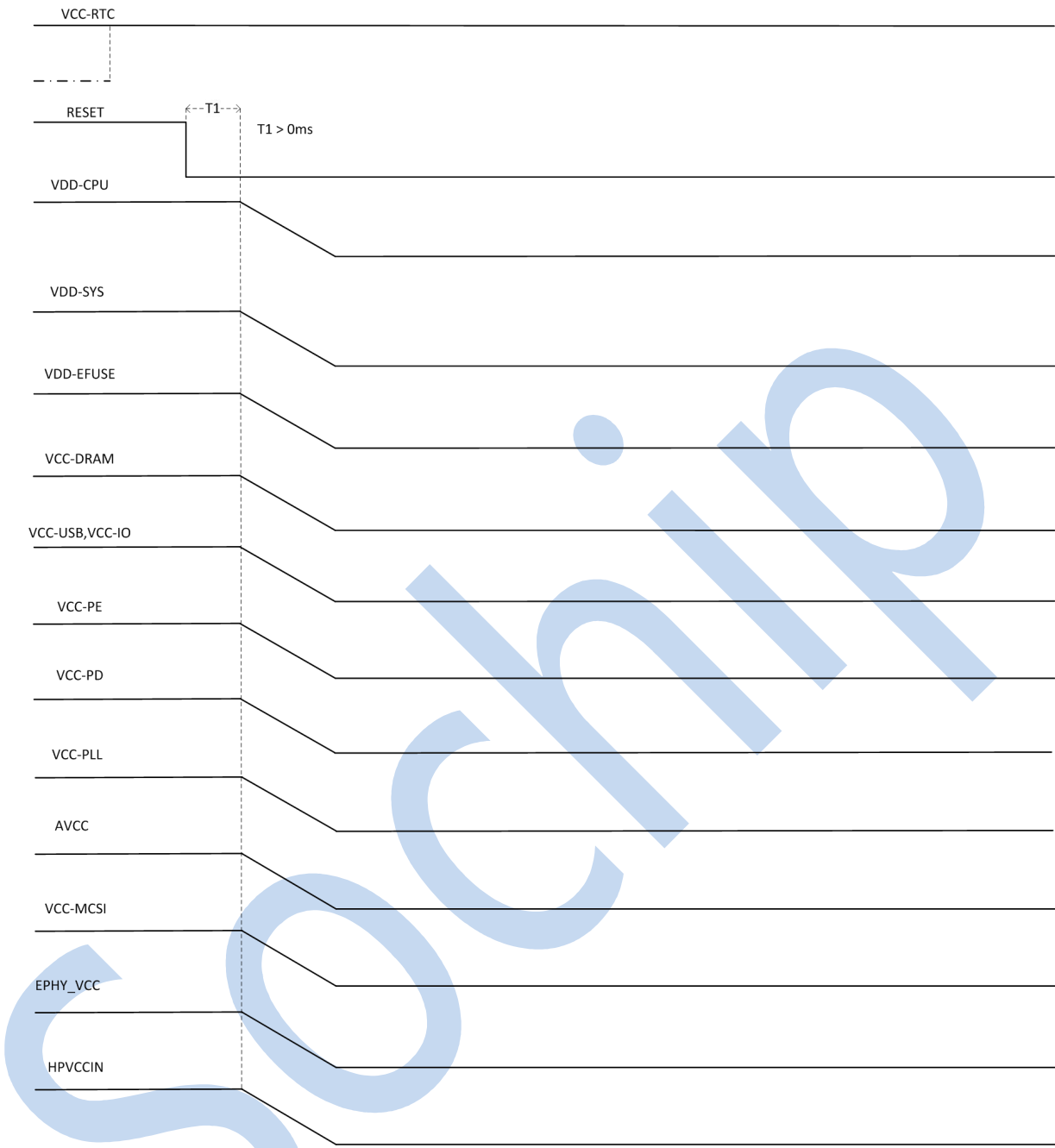


Figure 9-2. Power Down Sequence

Appendix

Pin Map

The following pin map shows the views of the 234-pin FBGA package of the S3 processor.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|--------------|--------------|--------------|--------------|-------------------|---------------|--------------|--------------|-------------|-------------|-------------|-------------|--------------|------|------|------|---|
| A | GND | PB13 | PC0 | | PB10 | | PB6 | | PD7 | | PD18 | | PD15 | PD13 | PD10 | GND | A |
| B | PC2 | PC1 | PB0 | PB1 | PB12 | PB8 | PB7 | PB2 | PD6 | PD21 | PD19 | PD16 | PD14 | PD12 | PD11 | PD4 | B |
| C | PC6 | PC3 | PC7 | PB3 | PB11 | PB9 | PB5 | PB4 | GND | PD20 | PD1 | PD17 | PE5 | PE2 | PD8 | PD5 | C |
| D | PC10 | PC9 | PC8 | GND | GND | GND | GND | GND | GND | GND | GND | GND | | PE17 | PE16 | | D |
| E | | EPHY_TX N | EPHY_TX P | GND | GND | GND | GND | GND | GND | GND | GND | PE6 | PE9 | GND | PE18 | PE19 | E |
| F | EPHY_R XN | EPHY_R XP | PC4 | PC5 | ZQ | VCC- DRAM | VCC- DRAM | VCC- DRAM | GND | GND | GND | PE4 | | PE0 | PE3 | | F |
| G | | MCSI- D0N | MCSI- D0P | GND | GND | GND | GND | VCC- DRAM | GND | GND | GND | VDD- CPU | PE1 | PE12 | PE7 | PE21 | G |
| H | MCSI- D1N | MCSI- D1P | GND | GND | GND | DVREF | GND | VCC- DRAM | GND | GND | VCC-IO | VDD- CPU | PE8 | PE11 | PE20 | | H |
| J | MCSI- CKN | MCSI- CKP | GND | GND | DZQ | GND | GND | VCC- DRAM | GND | GND | VDD- CPU | VDD- CPU | PE10 | PD2 | PD3 | PE22 | J |
| K | MCSI- D2N | MCSI- D2P | GND | GND | EPHY_LI NK_LED | GND | GND | VDD-SYS | VDD-SYS | GND | VDD- CPU | GND | PE15 | PE24 | PD0 | | K |
| L | | MCSI- D3N | MCSI- D3P | GND | EPHY_SP D_LED | VCC-PLL | GND | VDD-SYS | GND | GND | VCC-PD | VCC-PD | PE13 | PE23 | PD9 | PE14 | L |
| M | PF6 | PF5 | | VCC- MCSI | EPHY_V CC | VDD- EFUSE | AVCC | VDD-SYS | HPVCCB P | GND | VCC-PE | VCC-PE | PG13 | PG7 | PG6 | | M |
| N | | PF3 | PF4 | GND | EPHY_V DD | VCC-RTC | VCC-USB | GND | HBIAS | VRA2 | HPCOM FB | HPCOM | HPOUTR | PG8 | PG1 | PG3 | N |
| P | PF1 | PF2 | X32KFO UT | X24MO UT | VCC-IO | EPHY_R TX | RESET | AGND | MICIN3P | MBIAS | MICIN2 N | HPVCCI N | HPOUTL | PG11 | PG2 | PG0 | P |
| R | PF0 | USB-DM | X32KOU T | X24MIN | GND | LINEOUT L | NMI | LRADC1 | MICIN3 N | MICIN1 N | MICIN2P | LINEINL | JTAG_SE L | PG9 | PG4 | PG5 | R |
| T | GND | USB-DP | X32KIN | | RTC-VIO | LINEOUT R | | LRADC0 | | MICIN1P | | LINEINR | | PG10 | PG12 | GND | T |

Package Dimension

The following diagram shows the package dimension of the S3 processor.

